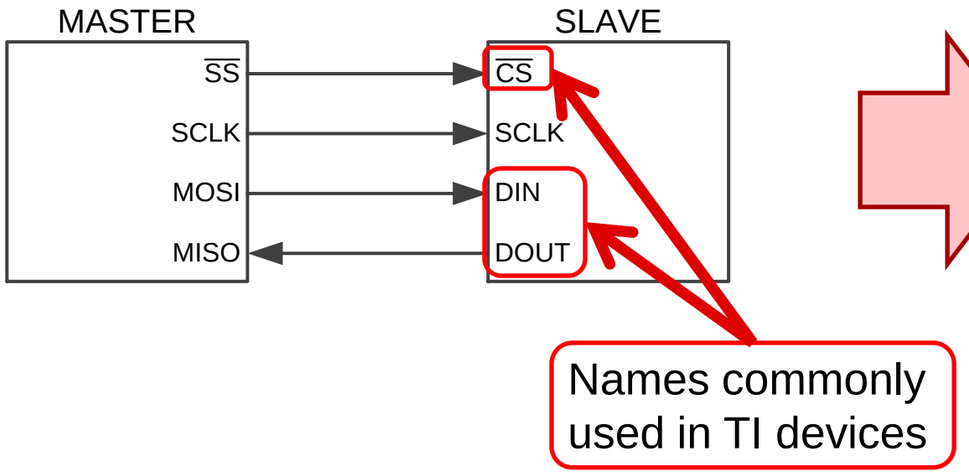
Basics of SPI: Timing Requirements and Switching Characteristics

TI Precision Labs – Digital Communications

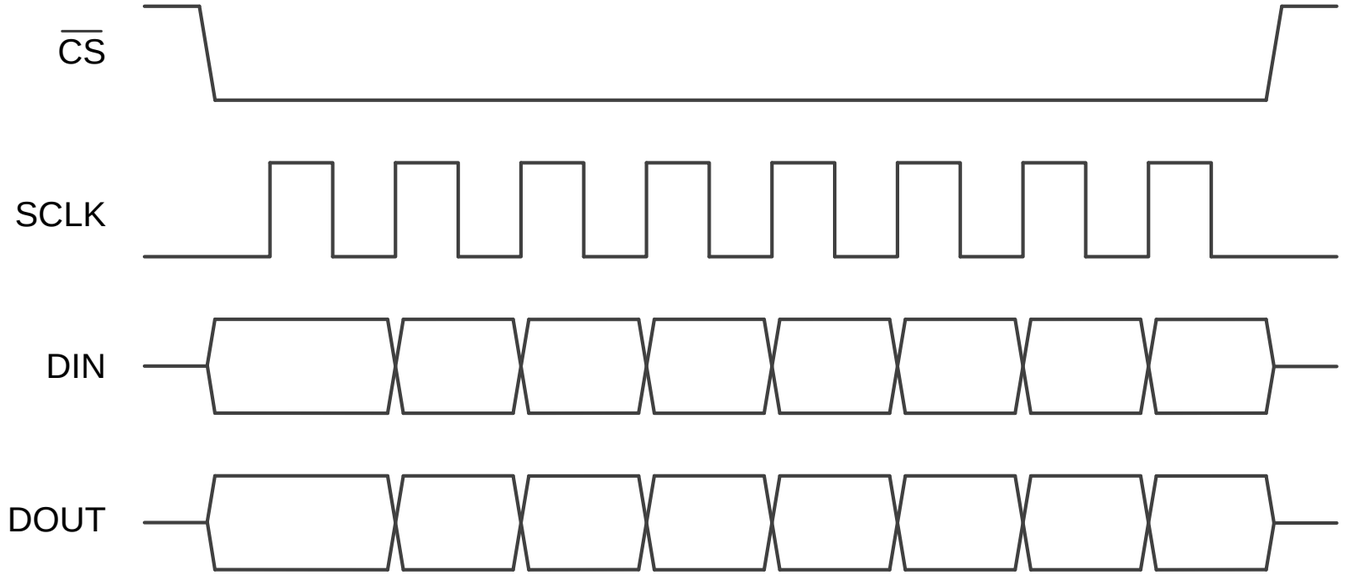
Presented by Alex Smith

Prepared by Joseph Wu

SPI Communication



A timing diagram shows the specifications and the timing relationship between the SPI digital lines



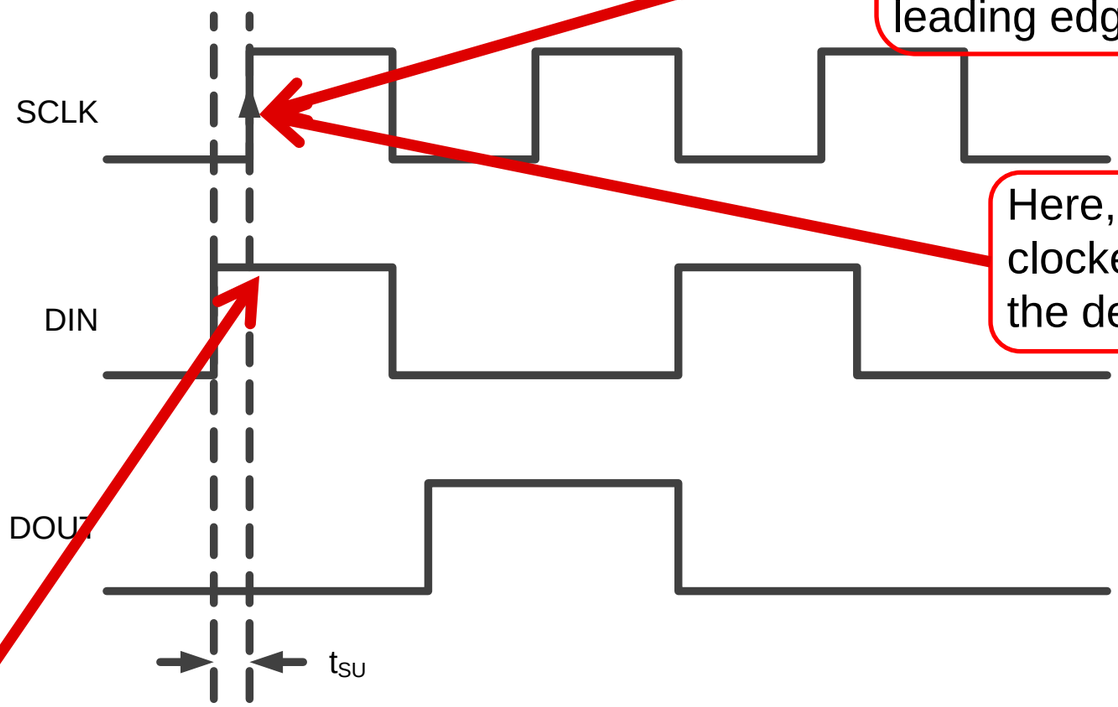
Violating a timing specification can cause a failure to read the data and may cause unexpected results.

SPI Timing: Setup Time

Setup time

Hold time

Propagation Delay



Example is SPI mode 0: SCLK idles low and data is clocked in on the leading edge of SCLK

Here, a 1 is clocked into the device

The state of DIN is read into the device at the rising edge of SCLK. To ensure the data is correctly read, DIN must be at the correct state for a setup time **before** the SCLK rises

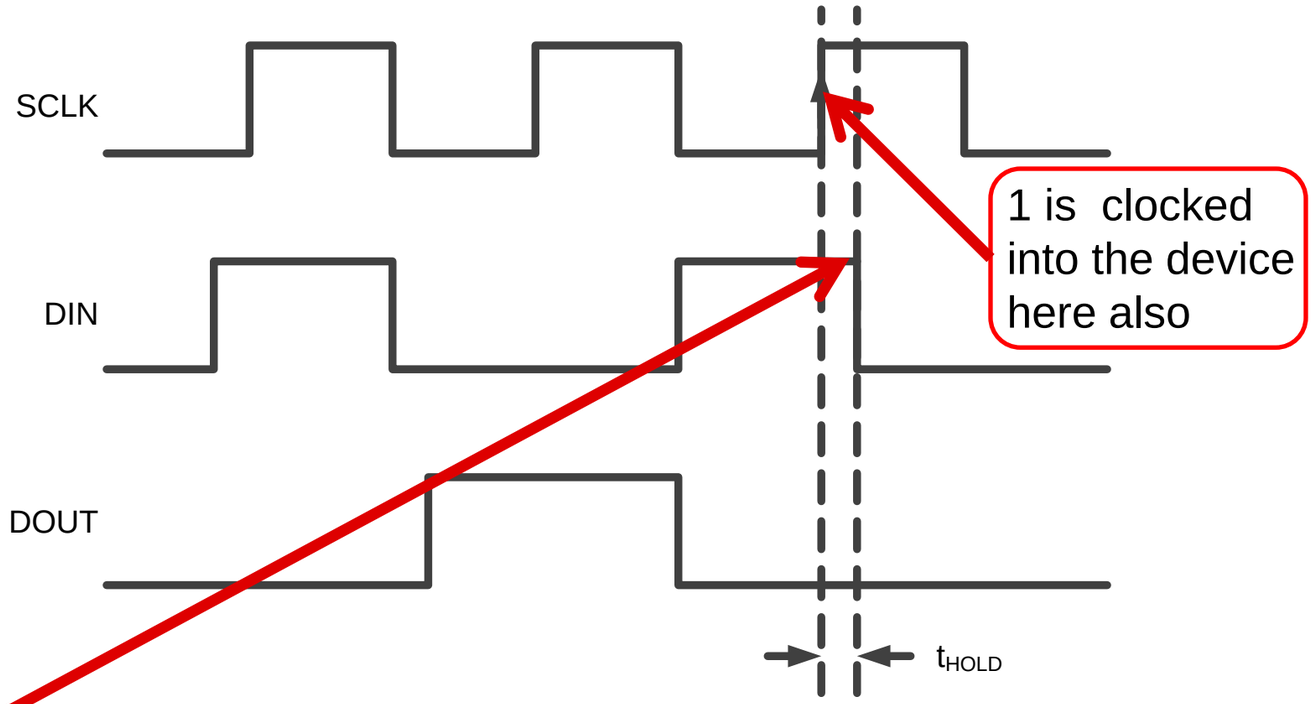
Setup time is the minimum time required before the clocking edge for which the data must be stable to be latched correctly

SPI Timing: Hold Time

Setup time

Hold time

Propagation Delay



Again, the state of DIN is read into the device at the rising edge of SCLK. DIN must be held at the correct state for a hold time **after** the SCLK rises

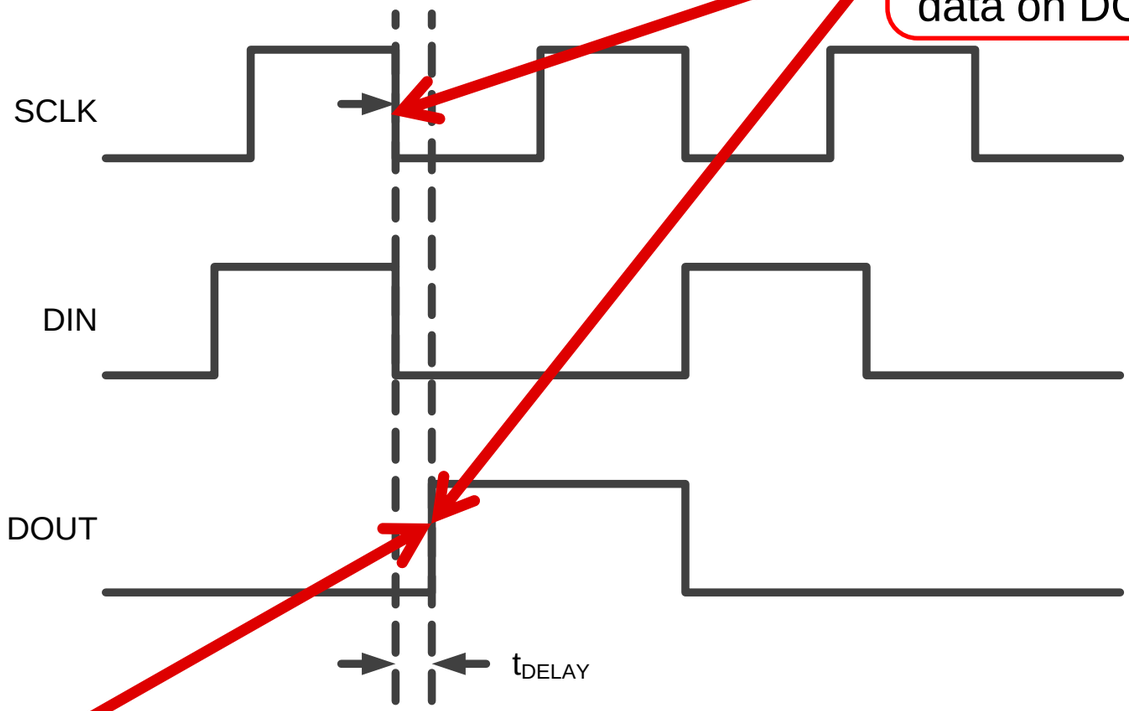
Hold time is the minimum time required after the clocking edge for which the data must be stable to be latched correctly

SPI Switching: Propagation Delay

Setup time

Hold time

Propagation Delay



The falling edge of SCLK sets up the data on DOUT

DOUT is read by the master at the rising edge of SCLK. However, the slave sets the output at the previous falling edge of SCLK. This delay from one clock event to the response is a propagation delay.

Propagation delay is the time required for an input change to cause an output change through the digital circuitry

SPI Timing

Timing Requirements and Switching Characteristics example from the ADS1118

Timing Requirements are typically setup times and hold times

7.6 Timing Requirements: Serial Interface

Over operating ambient temperature range and VDD = 2 V to 5.5 V (unless otherwise noted)

		MIN	MAX	UNIT
t_{CSSC}	Delay time, $\overline{CS}$ falling edge to first SCLK rising edge(1)	100		ns
t_{SCCS}	Delay time, final SCLK falling edge to $\overline{CS}$ rising edge	100		ns
t_{CSH}	Pulse duration, $\overline{CS}$ high	200		ns
t_{SCLK}	SCLK period	250		ns
t_{SPWH}	Pulse duration, SCLK high	100		ns
t_{SPWL}	Pulse duration, SCLK low(2)	100		ns
			28	ms
t_{DIST}	Setup time, DIN valid before SCLK falling edge	50		ns
t_{DIHD}	Hold time, DIN valid after SCLK falling edge	50		ns
t_{DOHD}	Hold time, SCLK rising edge to DOUT invalid	0		ns

(1) $\overline{CS}$ can be tied low permanently in case the serial bus is not shared with any other device.
(2) Holding SCLK low longer than 28 ms resets the SPI interface.

Switching Characteristics are typically propagation delays

7.7 Switching Characteristics: Serial Interface

Over operating ambient temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{CSDOD}	Propagation delay time, $\overline{CS}$ falling edge to DOUT driven	DOUT load = 20 pF || 100 kΩ to GND			100	ns
t_{DOPD}	Propagation delay time, SCLK rising edge to valid new DOUT	DOUT load = 20 pF || 100 kΩ to GND	0		50	ns
t_{CSDOZ}	Propagation delay time, $\overline{CS}$ rising edge to DOUT high impedance	DOUT load = 20 pF || 100 kΩ to GND			100	ns

SPI Timing Diagram

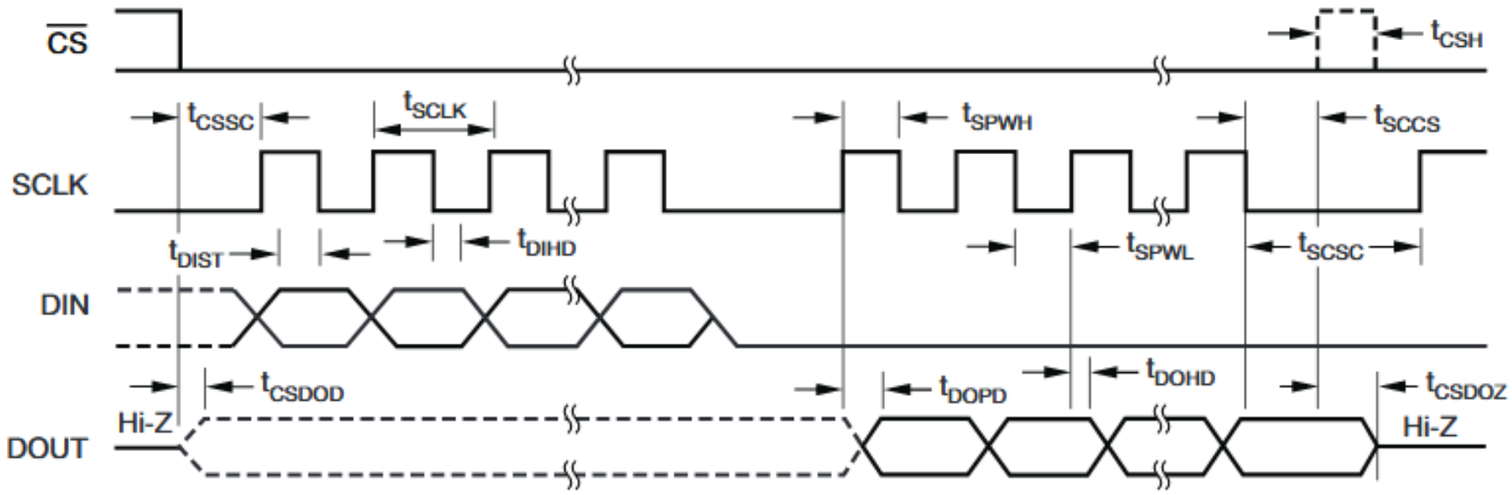


Figure 1. Serial Interface Timing

Timing diagram for the ADS1118

Device uses SPI Mode 1: SCLK idles low, data clocked in at falling edge of SCLK

Boxes for DIN and DOUT are high or low data

Arrows enclose timing specifications

SPI Timing Diagram

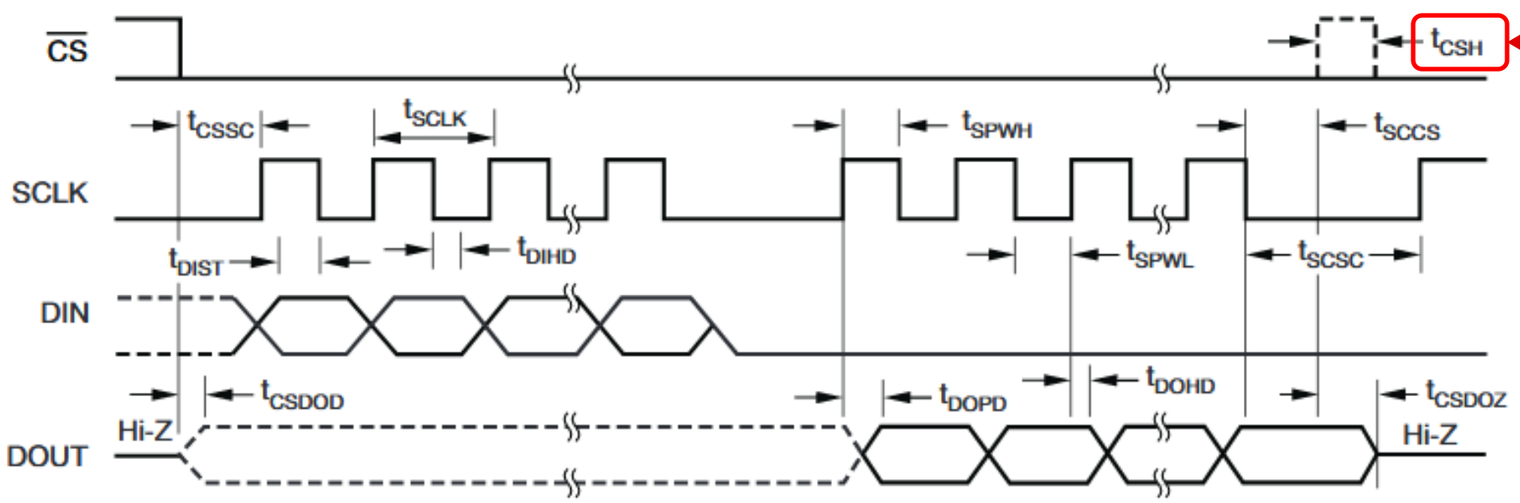


Figure 1. Serial Interface Timing

t_{CSH}

Minimum pulse duration, CS high

This time defines the time required for the CS to stay high to ensure that the device has reset the SPI communications.

SPI Timing Diagram

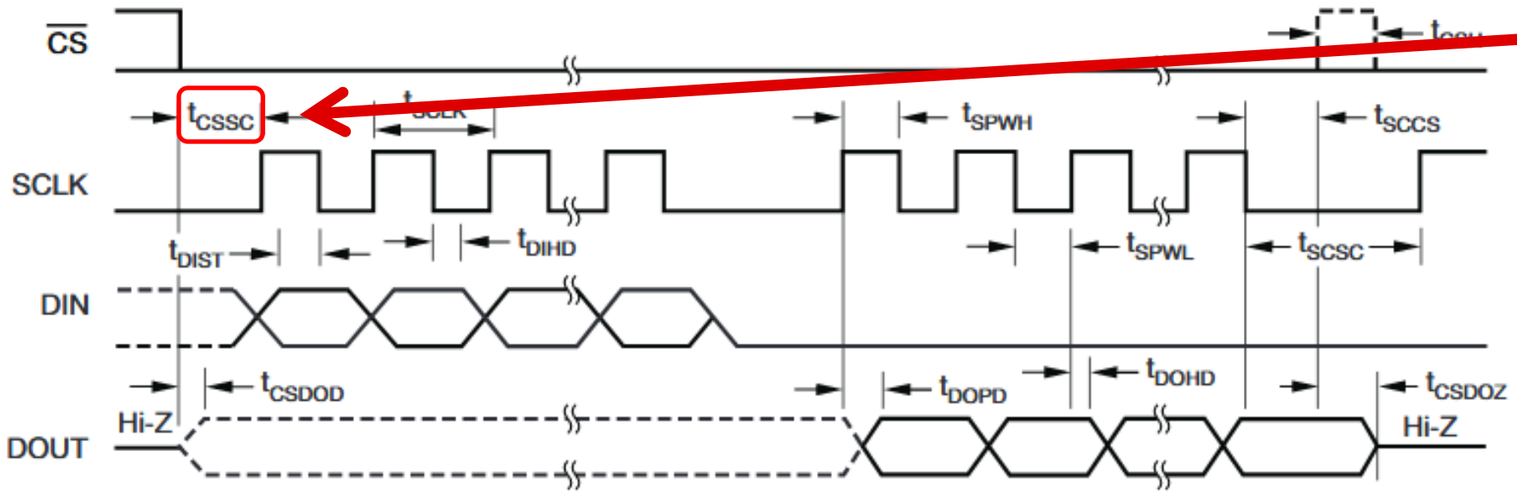


Figure 1. Serial Interface Timing

tcssc

CS low to first SCLK high

This time defines the time required for the CS to stay high to ensure that the device recognizes it is the slave.

A violation may cause the device to miss the first SCLK pulse

SPI Timing Diagram

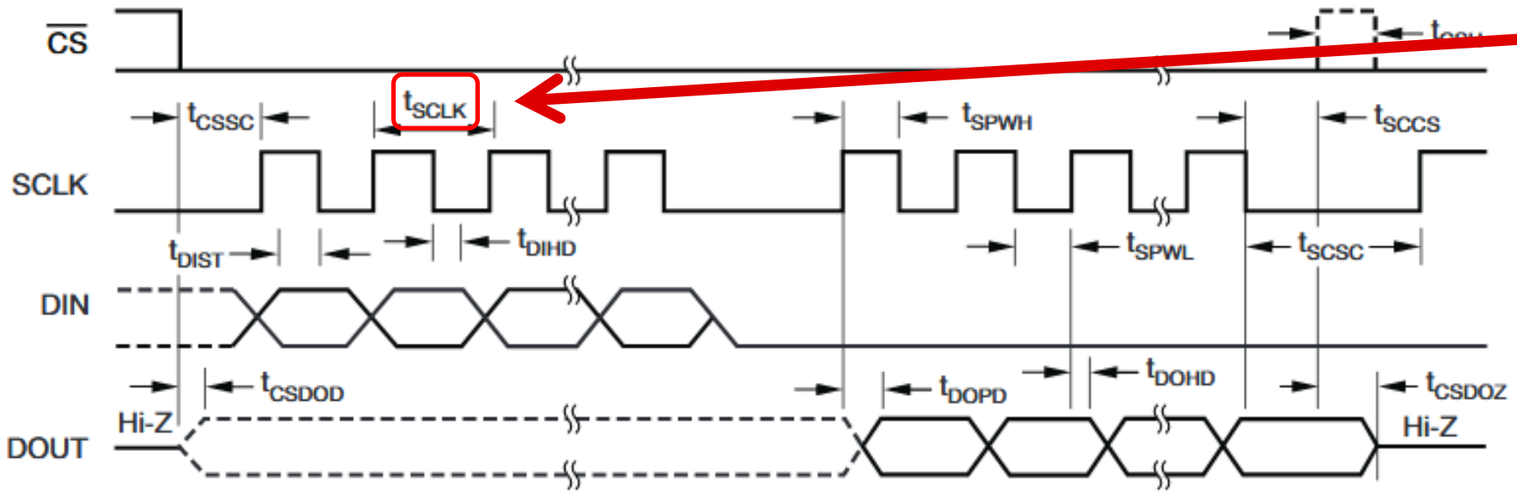


Figure 1. Serial Interface Timing

t_{SCLK}

The minimum time for an SCLK period

SCLKs can be sent to a device only so fast before the device fails to recognize it. This defines the minimum time for SCLK.

$1/t_{SCLK}$ is the SCLK frequency

SPI Timing Diagram

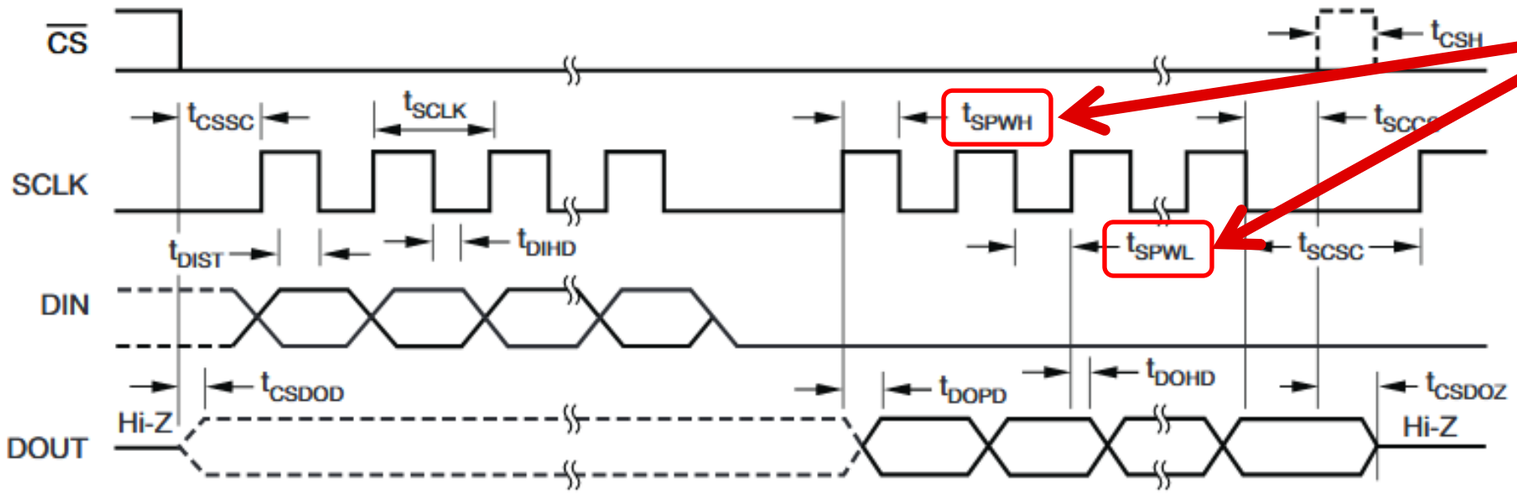


Figure 1. Serial Interface Timing

t_{SPWH}, t_{SPWH}

The minimum time for an SCLK high and the minimum time for an SCLK low

These two times with t_{SCLK} define how much skew in the SCLK duty cycle is allowed

For this device, there is a maximum t_{SPWL} for SPI timeout

SPI Timing Diagram

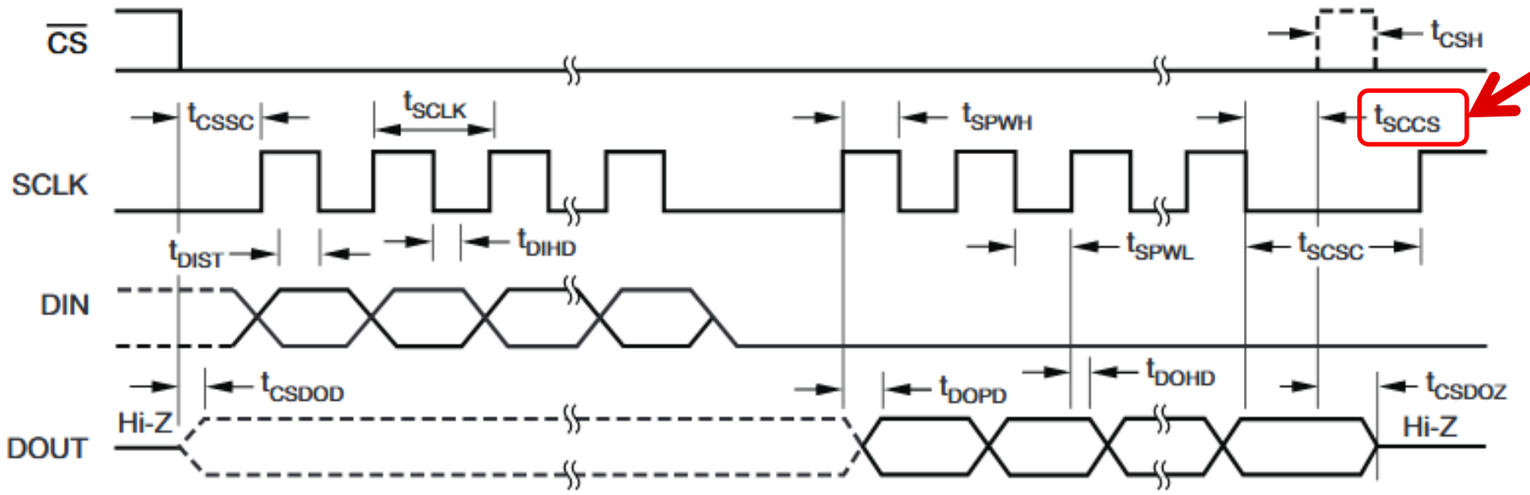


Figure 1. Serial Interface Timing

t_{SCCS}

Time from the falling edge of SCLK to the rising edge of CS

Because CS disables the SPI, ensure that the device receives the last bit of data before shutting down SPI communication

A violation of this could cause the device to miss the last data transmission

SPI Timing Diagram

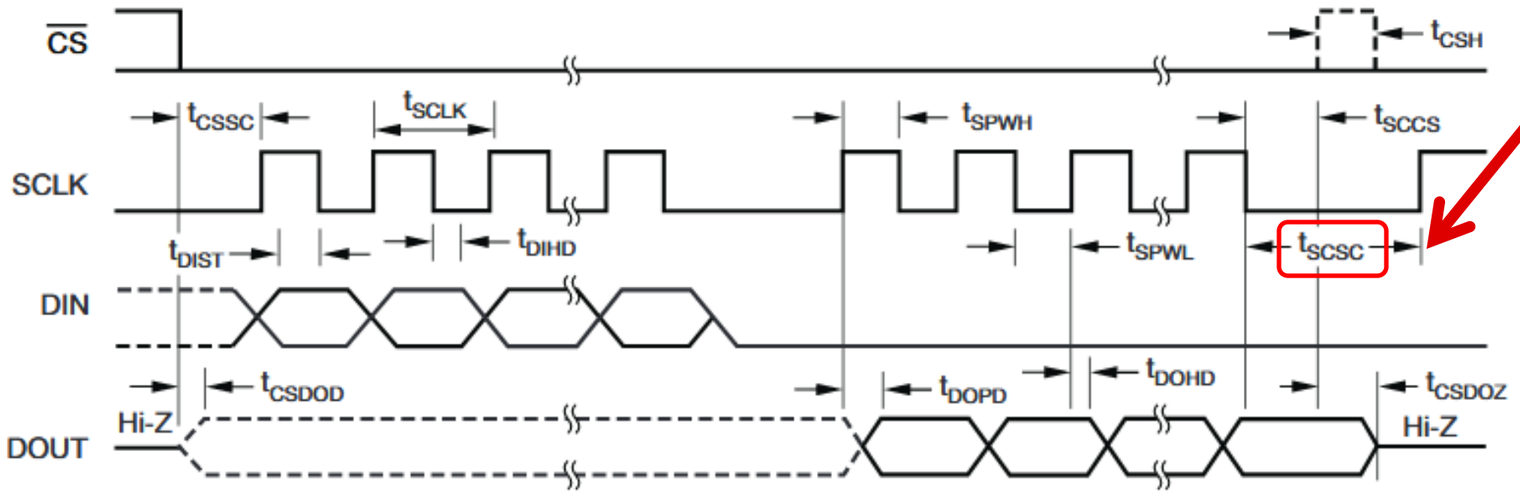


Figure 1. Serial Interface Timing

tscsc

Time from the falling edge of SCLK to the rising edge of SCLK in the next CS

This time is required to execute the command from one CS period, to start a new command in another CS period

SPI Timing Diagram

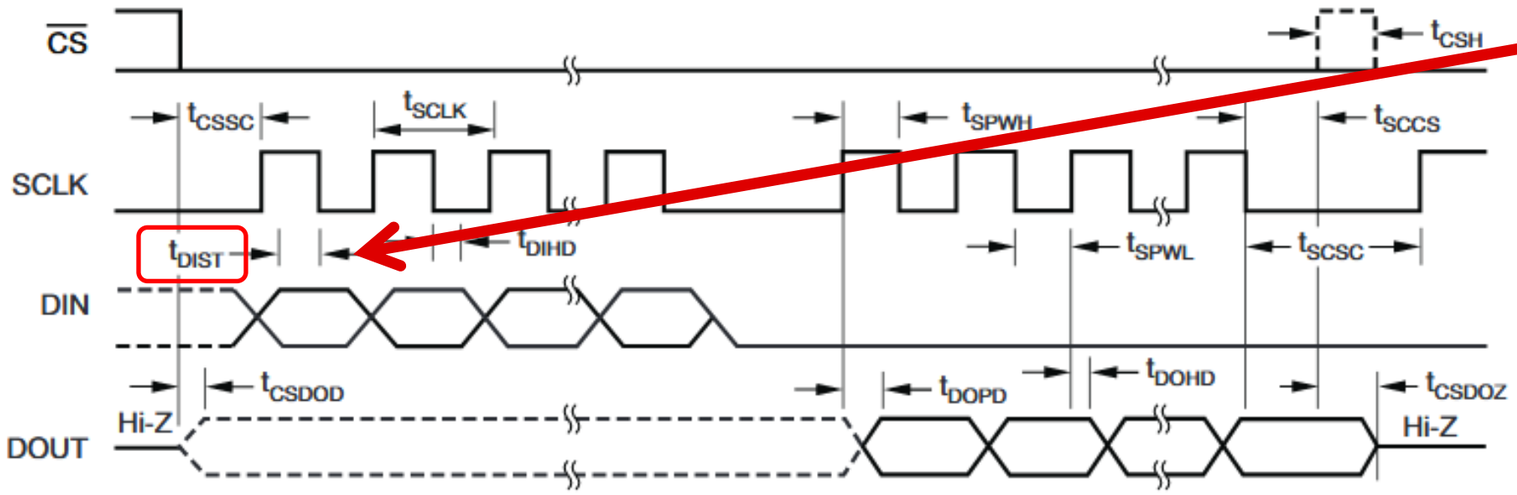


Figure 1. Serial Interface Timing

t_{DIST}

Setup time from the rising edge of DIN to the falling edge of SCLK

For data to be read into the device, the DIN must first be established for a time period before the SCLK falling edge.

SPI Timing Diagram

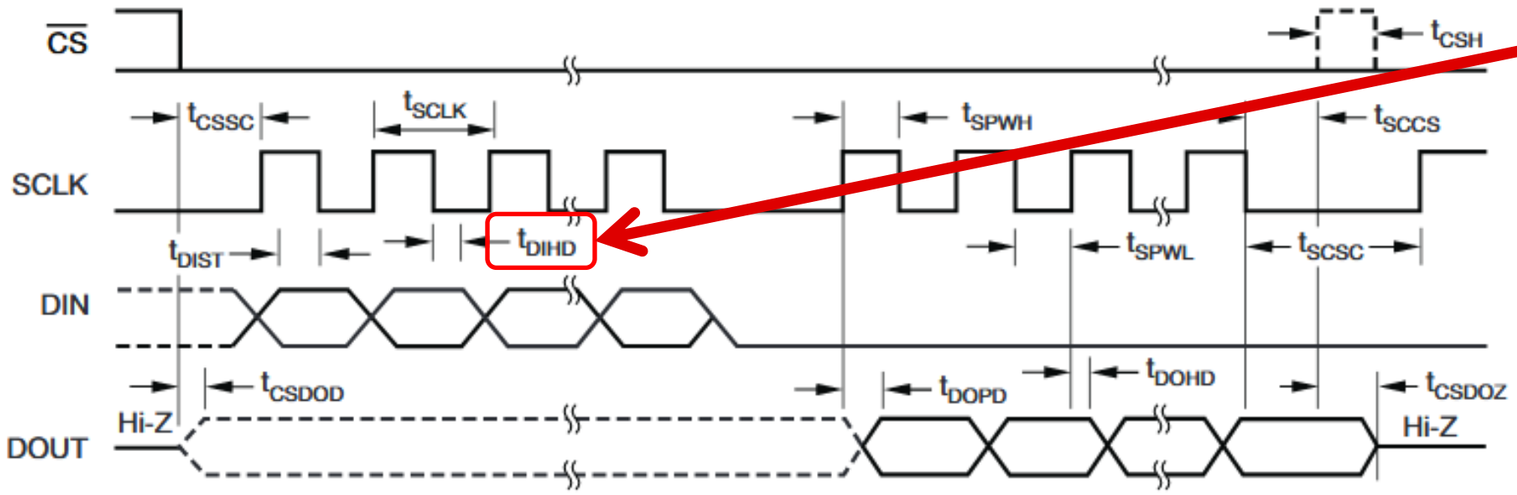


Figure 1. Serial Interface Timing

t_{DIHD}

Hold time from the falling edge of SCLK to the falling edge of DIN.

Once the data is set onto the DIN line, the SCLK falling edge latches the data into the device. However, there is a required time for the data to be held after the SCLK falling edge

SPI Timing Diagram

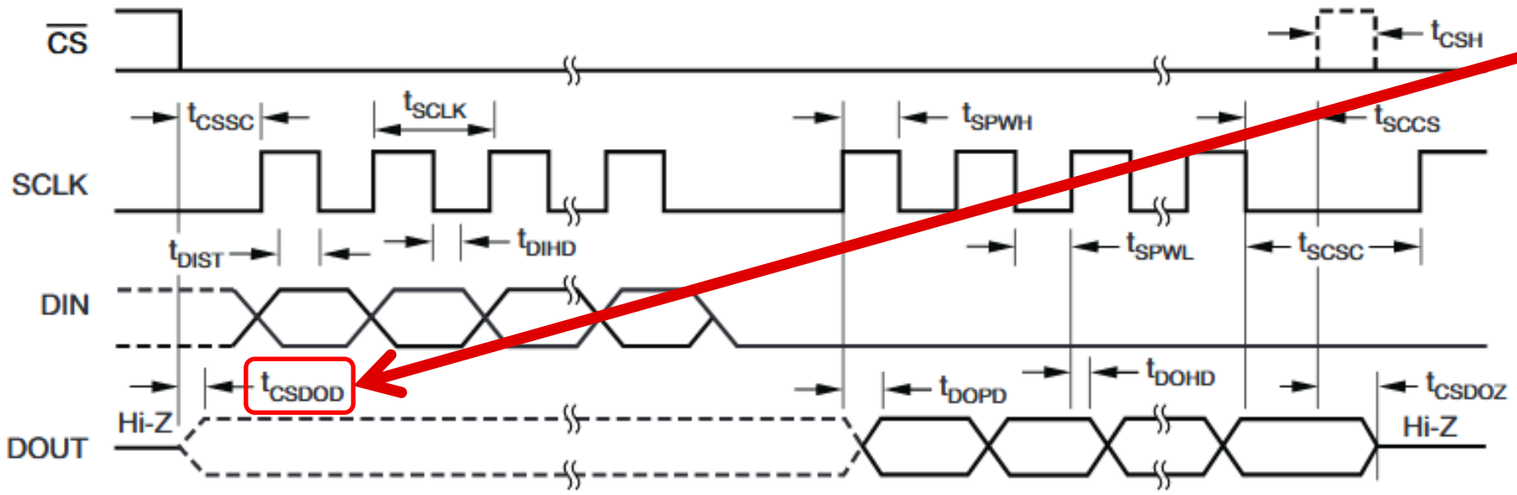


Figure 1. Serial Interface Timing

t_{CSDOD}

Propagation delay time from CS falling to DOUT actively driven

When CS is high, the DOUT is high impedance or Hi-Z, allowing for multiple devices on the bus to drive DOUT a device at a time.

When CS goes low, DOUT is actively driven

SPI Timing Diagram

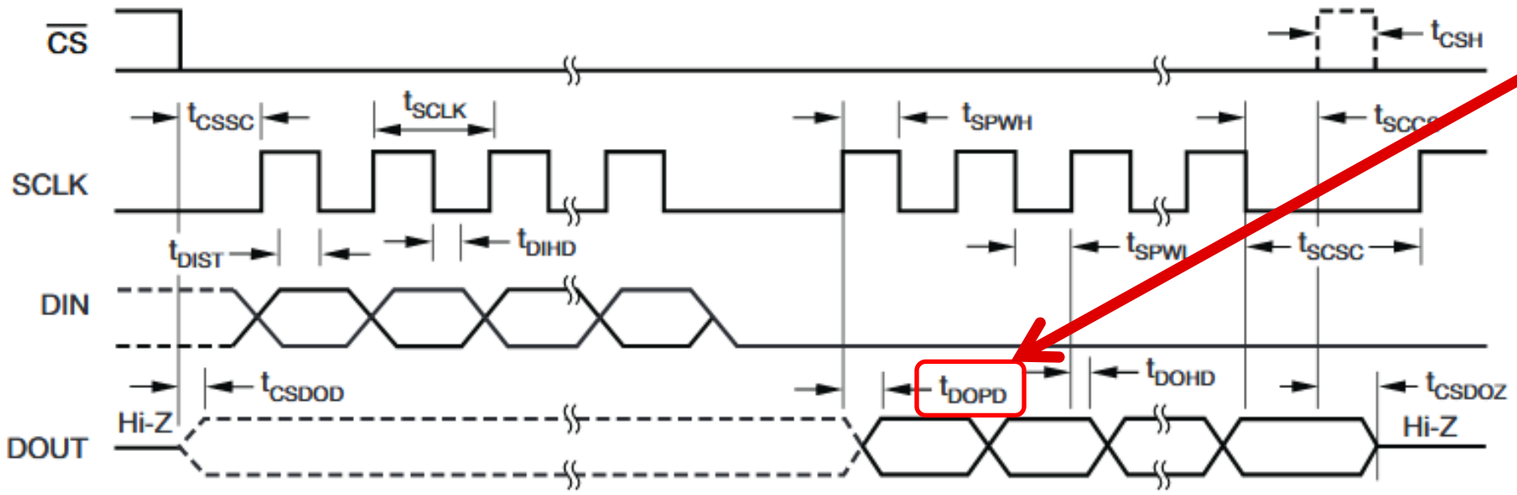


Figure 1. Serial Interface Timing

t_{DOPD}

Propagation delay time from rising edge of SCLK to data appearing on DOUT

SCLK is used to clock out data from the device. When SCLK is driven high, this signals to the device that data should be put on DOUT that can be clocked out on the falling edge of DOUT

SPI Timing Diagram

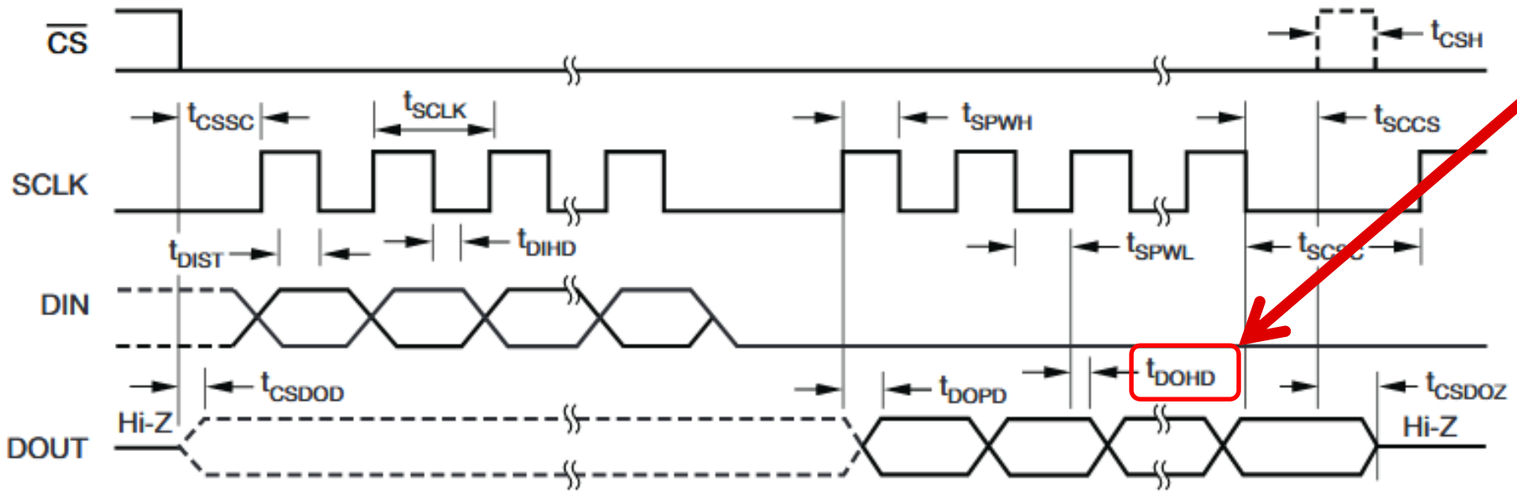


Figure 1. Serial Interface Timing

t_{DOHD}

Propagation delay time from rising edge of SCLK to data changing on DOUT

This defines the time for which the last data is still valid once the rising edge of SCLK occurs

SPI Timing Diagram

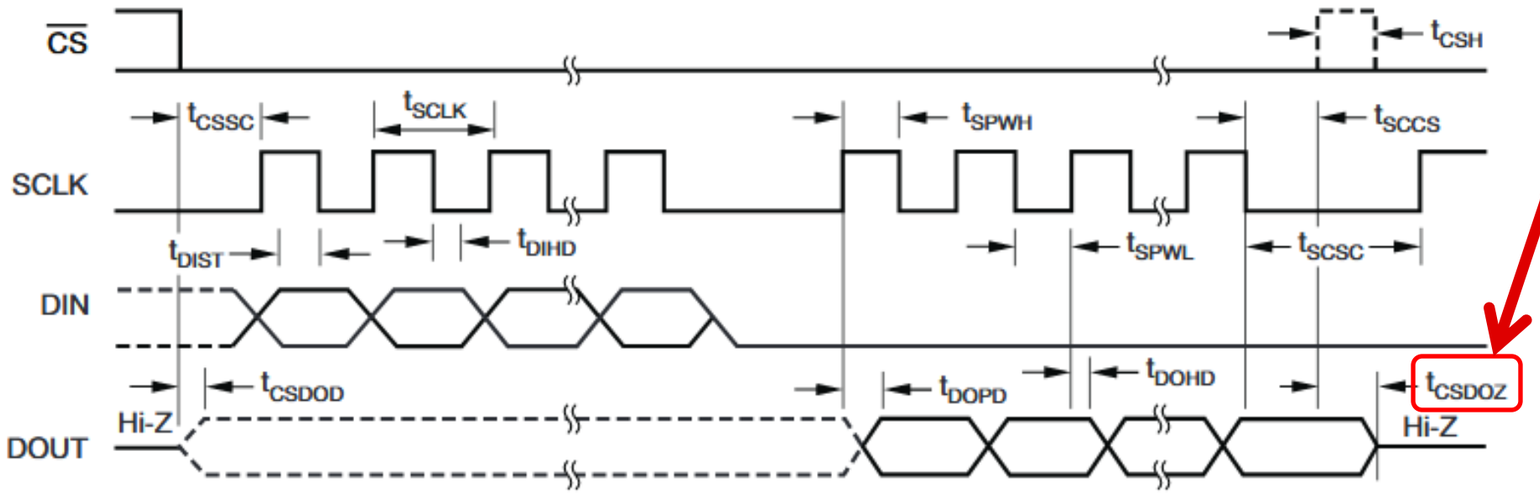


Figure 1. Serial Interface Timing

t_{CSDOZ}

Propagation delay time from rising edge of CS to DOUT becoming Hi-Z

Thanks for your time!
Please try the quiz.

Quiz: Basics of SPI: Timing Requirements and Switching Characteristics

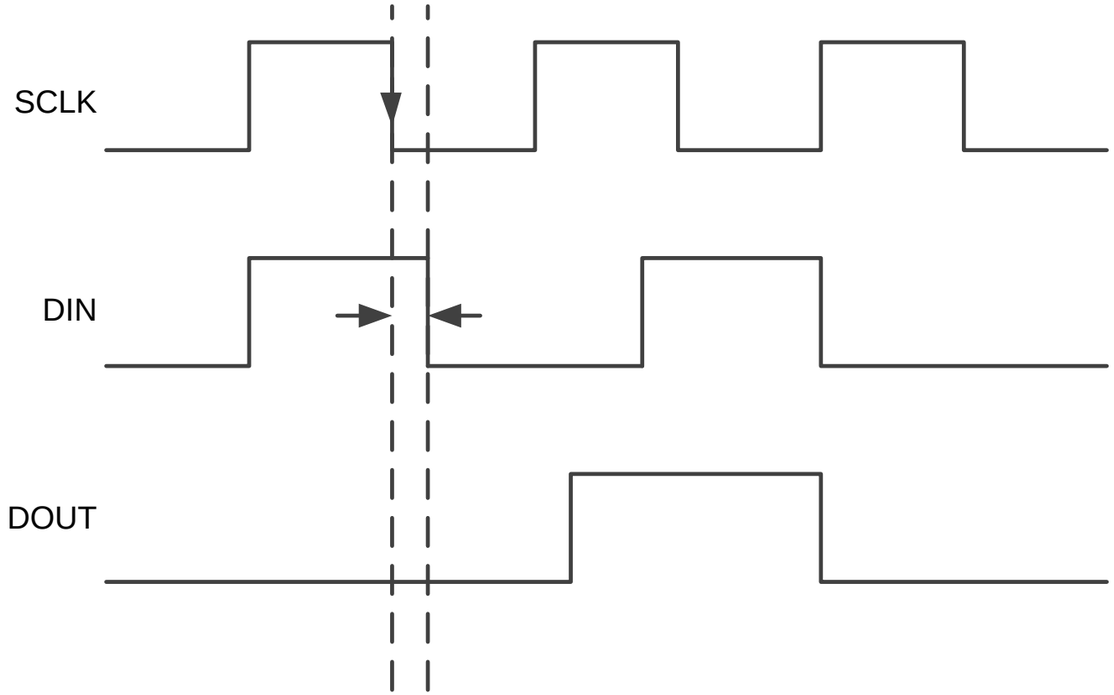
TIPL xxxx

TI Precision Labs – Precision Data Converters

Created by Joseph Wu

Quiz: Basics of SPI: Timing Diagram

1. The following diagram is CPOL = 0, CPHA = 1. Data is clocked in on the falling edge of SCLK. DIN must be stable for a time after the SCLK falling edge. This timing is an example of which timing requirement?
   a. Setup time
   b. Hold time
   c. Propagation delay
   d. None of the above



Quiz: Basics of SPI: Timing Diagram

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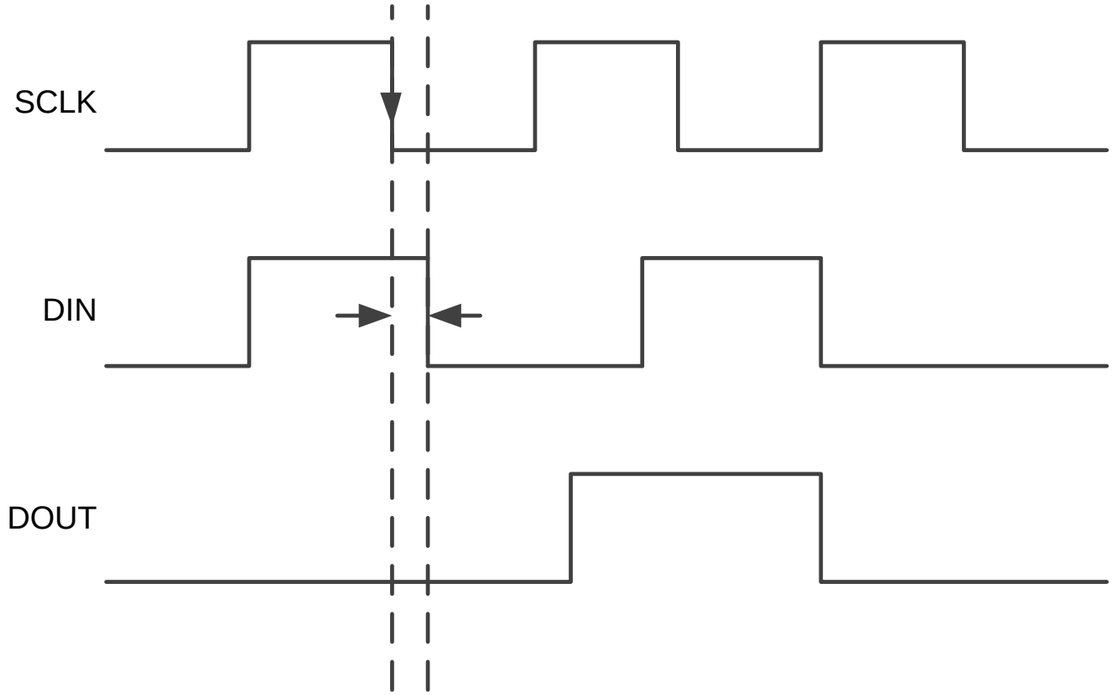

Quiz: Basics of SPI: Timing Diagram

2. The following diagram is CPOL = 0, CPHA = 1. DIN and DOUT are read on the falling edge of SCLK. However, DOUT is set up on the rising edge of SCLK, and there may be time required for the data to arrive on DOUT. This timing is an example of which timing requirement?

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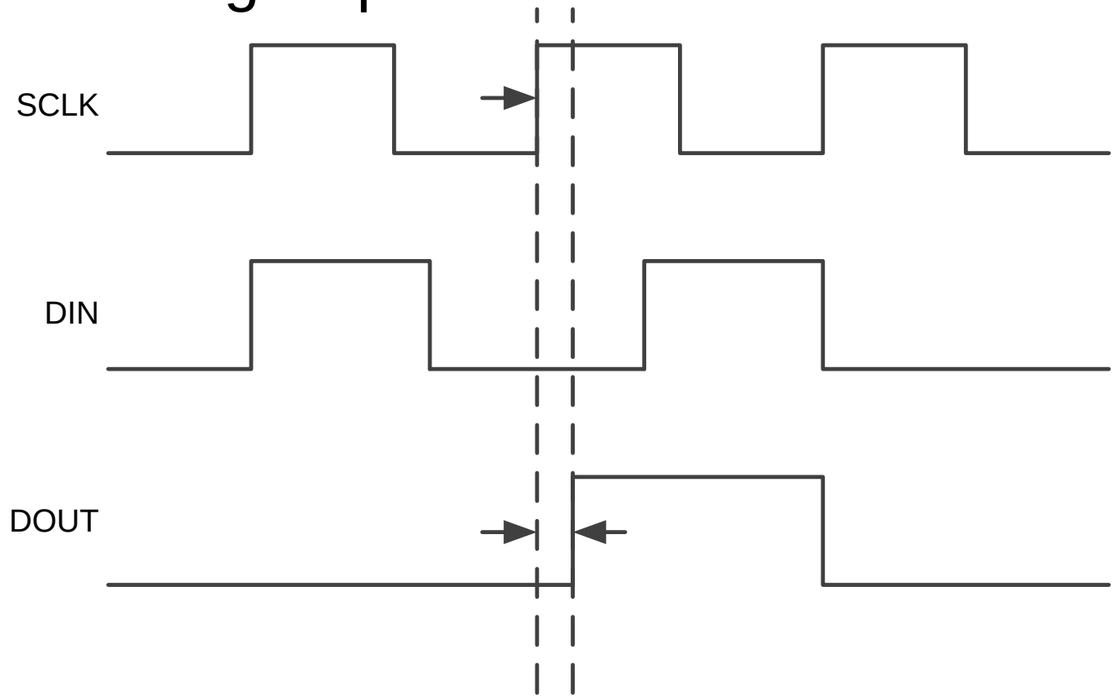

Quiz: Basics of SPI: Timing Diagram

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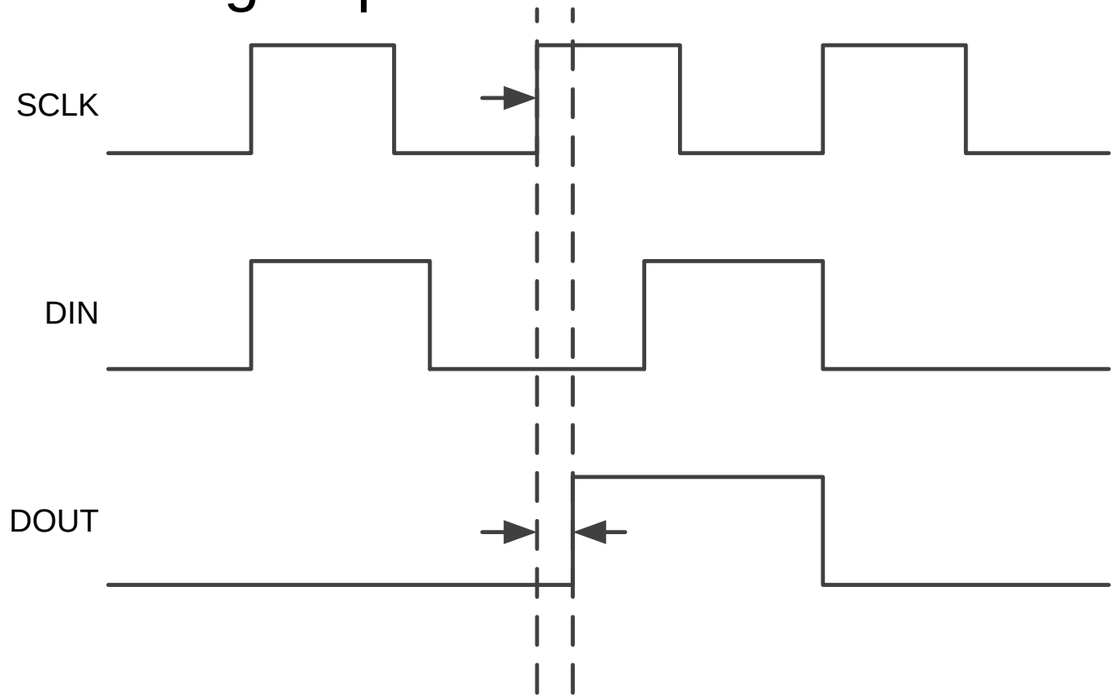

Quiz: Basics of SPI: Timing Diagram

3. The following diagram is CPOL = 0, CPHA = 1. Data is clocked in on the falling edge of SCLK. DIN must be stable for a time before the falling edge of SCLK. This timing is an example of which timing requirement?
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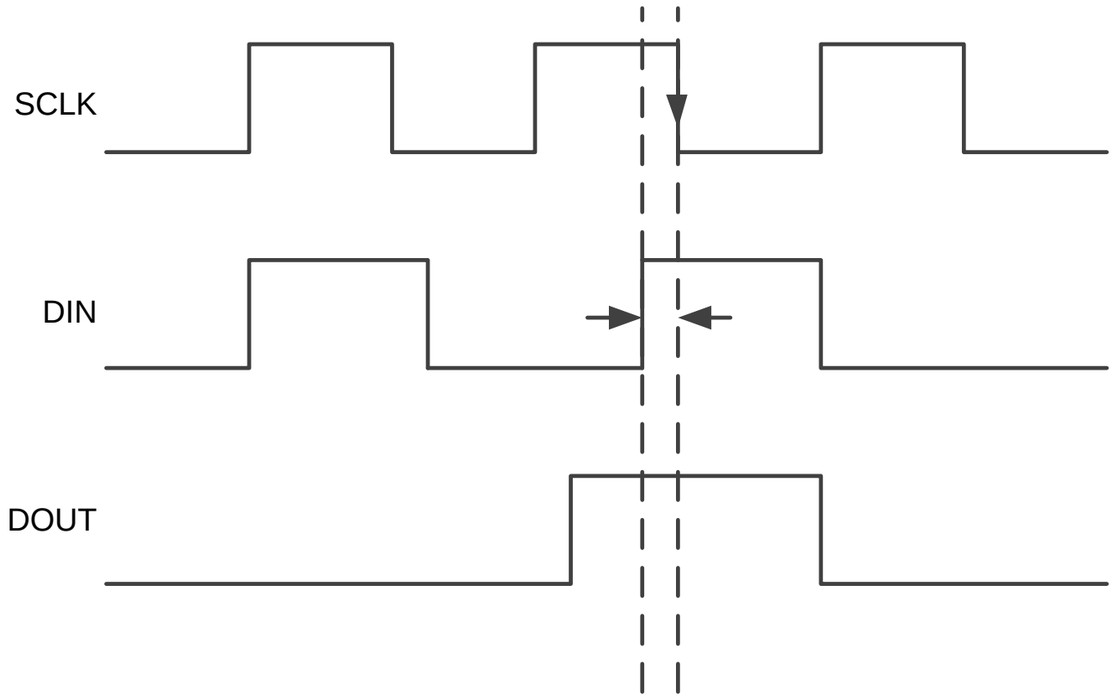
   b. Hold time
   c. Propagation delay
   d. None of the above



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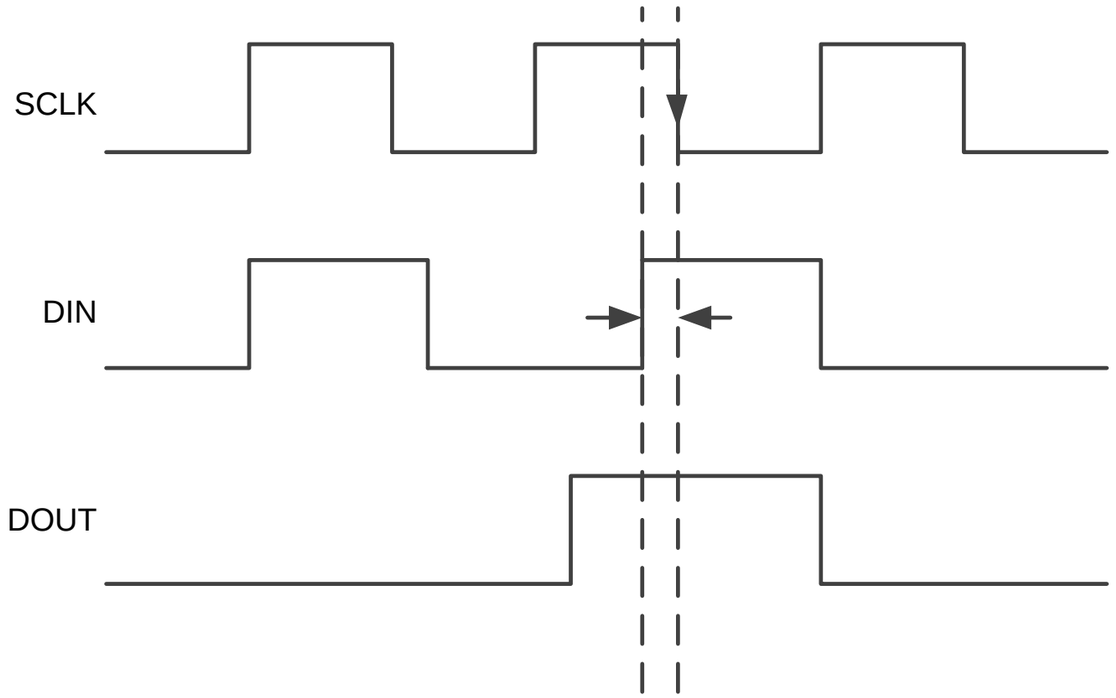

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