Module 4

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Field Effect Transistors

Module 4.1
Junction Field Effect Transistors

What you´ll learn in Module 4

Field Effect Transistors

Although there are lots of confusing names for field effect transistors (FETs) there are basically two main types:

1. The reverse biased PN junction types, the JFET or Junction FET, (also called the JUGFET or Junction Unipolar Gate FET).

2. The insulated gate FET devices (IGFET).

All FETs can be called UNIPOLAR devices because the charge carriers that carry the current through the device are all of the same type i.e. either holes or electrons, but not both. This distinguishes FETs from the bipolar devices in which both holes and electrons are responsible for current flow in any one device.

The JFET

This was the earliest FET device available. It is a voltage-controlled device in which current flows from the SOURCE terminal (equivalent to the emitter in a bipolar transistor) to the DRAIN (equivalent to the collector). A voltage applied between the source terminal and a GATE terminal (equivalent to the base) is used to control the source - drain current. The main difference between a JFET and a bipolar transistor is that in a JFET no gate current flows, the current through the device is controlled by an electric field, hence "Field effect transistor". The JFET construction and circuit symbols are shown in Figures 1, 2 and 3.

JFET Construction

The construction of JFETs can be theoretically quite simple, but in reality difficult, requiring very pure materials and clean room techniques. JFETs are made in different forms, some being made as discrete (single) components and others, using planar technology as integrated circuits.

Fig. 4.1.1 shows the (theoretically) simplest form of construction for a Junction FET (JFET) using diffusion techniques. It uses a small slab of N type semiconductor into which are infused two P type areas to form the Gate. Current in the form of electrons flows through the device from source to drain along the N type silicon channel. As only one type of charge carrier (electrons) carry current in N channel JFETs, these transistors are also called "Unipolar" devices.

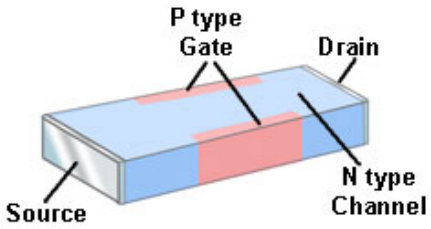

Fig. 4.1.1 Diffusion JFET Construction

Fig. 4.1.2 shows the cross section of a N channel planar Junction FET (JFET) The load current flows through the device from source to drain along a channel made of N type silicon. In the planar device the second part of the gate is formed by the P type substrate.

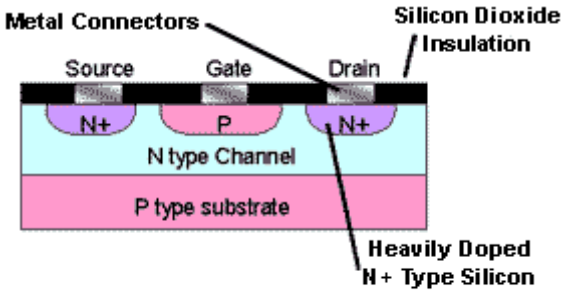

Fig. 4.1.2 JFET Planar Construction

JFET Circuit Symbols

P channel JFETs are also available and the principle of operation is the same as the N channel type described here, but polarities of the voltages are of course reversed, and the charge carriers are holes.

Notice in the JFET circuit symbols shown in Fig. 4.1.3 that the arrowhead on the gate connection always points towards the negative connection, indicating the polarity (either P or N channel) of the channel.

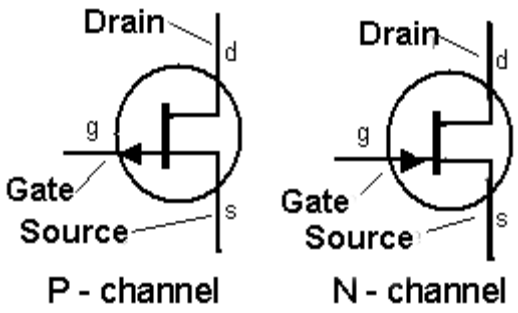

Fig. 4.1.3 JFET Circuit symbols

Module 4.2
How a JFET Works

What you'll learn in Module 4

- Operation Below Pinch Off.
- Operation Above Pinch Off.
- JFET Output Characteristic.
- JFET Transfer Characteristic.
- JFET Video.

The JFET is a Voltage Controlled Transistor.

The JFET is a voltage controlled transistor that has two distinct areas of operation depending on the whether the voltage applied to the Source and Drain terminals is greater or less that the transistor's Pinch-Off Voltage

The Pinch Off Voltage

The Pinch-Off value of the JFET refers to the voltage applied between Drain and Source (with the Gate voltage at zero volts) at which maximum current flows. Operating with the Drain/Source voltage below this value is classed is the "Ohmic Region" as the JFET will act rather like a resistor. Operating with the Drain Source voltage above Pinch Off is known as the "Saturation Region" as the JFET is acting like a saturated transistor; that is any increase in voltage does not produce a relative increase in current.

Operation Below Pinch Off

In the planar construction N channel JFET shown in Fig. 4.2.1, the N channel is sandwiched between two P type regions (the gate and the substrate) that are connected together and are at 0V. This forms the gate. The N type channel is connected to the source and drain terminals via more heavily doped N+ type regions. The drain is connected to a positive supply, and the source to zero volts. N+ type silicon has a lower resistivity than N type. This gives it a lower resistance, increasing conduction and reducing the effect of placing standard N type silicon next to the aluminium connector, which because aluminium is a tri-valent material, having three valence electrons whilst silicon has four, would tend to create an unwanted junction, similar in effect to a PN junction at this point.

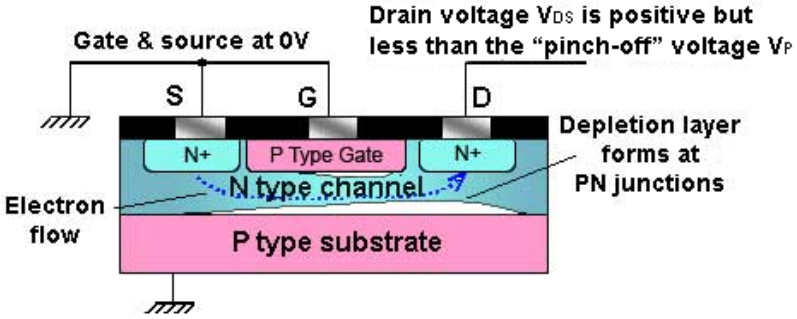

Fig. 4.2.1 JFET Operation Below "Pinch Off"

The P type gate is at 0V and is therefore negatively biased compared to the channel, which has a potential gradient on it, as one end is connected to 0 volts (the source), and the other end to a positive voltage (the drain). Any point on the channel (apart from the extreme end near the source terminal) must therefore be more positive than the gate. Therefore the two PN junctions formed between the N type conducting channel and the P type areas of the gate/substrate are both reverse biased, and so have a depletion layer that extends into the channel as shown in Fig. 4.2.1.

The shape of the depletion layer is not symmetrical, as can be seen from Fig. 4.2.1. It is generally thicker towards the drain end of the channel, because the voltage on the drain is more positive than that on the source due to the voltage gradient that exists along the channel. This causes a larger potential across the junctions nearer the drain, and so a thickening of the depletion layer. The effect becomes more marked when the voltage between drain and source is greater than about 1 volt or so.

Operation Above "Pinch Off"

When a voltage is applied between drain and source (V_{DS}) current flows and the silicon channel acts rather like a conventional resistor (The Ohmic Region). Now if V_{DS} is increased (with VGS held at zero volts) towards what is called the pinch off value V_P, the drain current I_D also at first, increases. The transistor is working in the "ohmic region" as shown in Fig. 4.2.1.

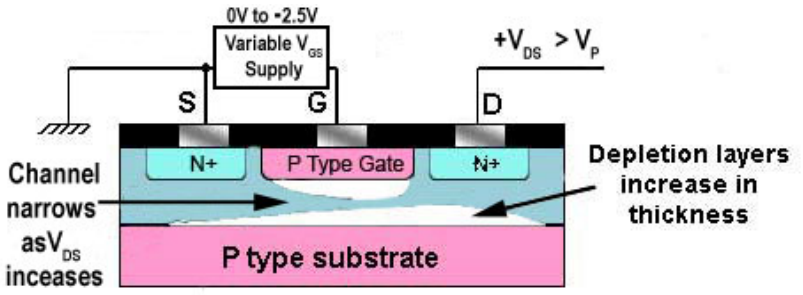

Fig. 4.2.2 JFET Operation Above "Pinch Off"

However as drain source voltage V_{DS} increases, the depletion layers at the gate junctions are also becoming thicker and so narrowing the N type channel available for conduction. There comes a point, (Pinch Off) where the conducting channel has become narrow enough to cancel out the effect of current increasing with the applied voltage V_{DS} as shown in fig 4.2.2. Above this (Pinch Off) point there is little further increase in drain current and the transistor is said to operating in the "Saturation Region".

However, if the JFET is biased with V_{DS} at Pinch Off voltage (V_P) a small change in V_{GS} can be used to control the current through the source-drain channel from zero current to its maximum (saturated)value .

JFET Characteristics

This type of operation is shown in the fairly flat top to the output characteristics shown in Fig 4.2.3. Notice that each curve is drawn for a particular value of negative voltage between gate and source, and that when sufficient reverse bias is applied to the gate (e.g. more than -2.5V, the lowest value on the graph) the drain current ceases completely.

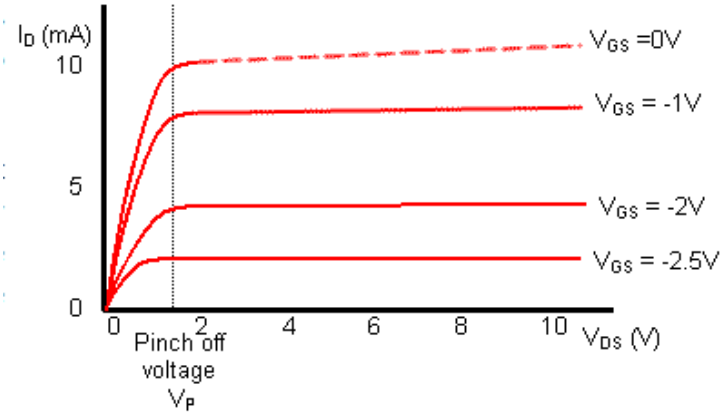

Fig. 4.2.3 JFET Output Characteristic

In the JFET output characteristics shown in Fig. 4.2.3, the Drain current I_D increases in a linear manner (like a resistor) at values of Gate/Source voltage (V_{GS}) below pinch off (The Ohmic Region), but above V_P (The Saturation Region) shows very little change, and the curves are very nearly horizontal at voltages greater than the pinch off voltage (V_P). Almost all of the expected increase in current, due to the increase in voltage between Source and Drain (VDS), is offset by the narrowing of the conducting channel due to the growing depletion layers.

The tranconductance characteristic for a JFET, which shows the change in Drain current (I_D) for a given change in Gate-Source voltage (V_{GS}), is shown in Fig 4.2.4. Because the JFET input (the Gate) is voltage operated, the gain of the transistor cannot be called current gain, as with bipolar transistors. The drain current is controlled by the Gate-Source voltage, so the graph shows milli-amperes per volt (mA / V), and as current divided by Voltage (I/V) is CONDUCTANCE (the inverse of resistance (V/I) the slope of this graph (the gain of the device) is called the FORWARD or MUTUAL TRANSCONDUCTANCE, which has the symbol gm. Therefore the higher the value of gm the greater the amplification.

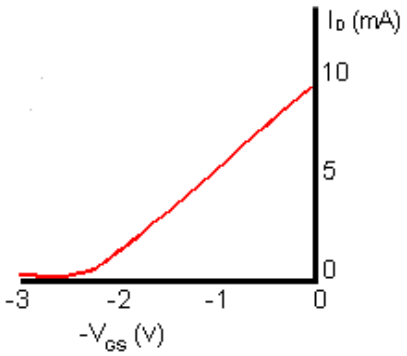

Fig. 4.2.4 JFET Transconductance Characteristic

Notice that V_{GS} is always shown as being negative; in reality it may be zero or slightly above zero, but the gate is always more negative than the N type channel between source and drain. Note also that the slope of the curve in the transfer characteristic is less steep than that of the Mutual Conductance characteristic for a typical bipolar transistor (compare Fig. 4.2.4 and Fig. 3.5.4 on the Bipolar Transistors Current Gain page). This means that a JFET will have a lower gain than that of a bipolar transistor.

This disadvantage is offset by the advantage of having an extremely high input resistance. A typical input resistance for a JFET would be in the region of 1 x 10^{10} ohms (10,000 Megohms!) compared with 2K to 3K Ohms for a bipolar device.

This makes the JFET ideal for applications where the circuit or device driving the JFET amplifier cannot supply any appreciable current, an example being the Electret microphone, which uses a FET within the microphone to amplify the tiny voltage variations appearing across the vibrating diaphragm element.

Another feature of the JFET that makes it more suited to very high frequency use than bipolar transistors, is the absence of junctions in the JFET conducting channel. In a bipolar transistor two PN junctions forming tiny capacitances, exist between base and emitter, and base and collector, due to the PN junctions. These capacitances will limit high frequency performance, as they provide negative feedback paths at high frequencies. Because the JFET is in effect just a slab of silicon between Source and Drain, the stray capacitances that exist in bipolar devices are absent, so high frequency performance is improved, making JFETs usable even at hundreds of MHz.

Download a datasheet for a typical N Channel JFET from On Semiconductor

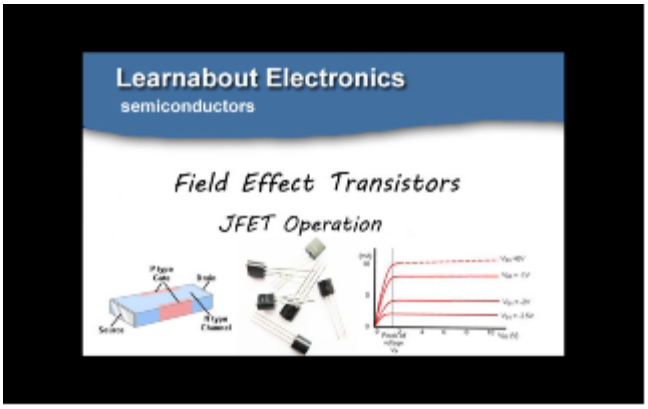

Fig 4.2.5 JFET Operation

Video is available at https://learnabout-electronics.org/Semiconductors/fet_02.php

Module 4.3
Enhancement Mode MOSFETs.

What you'll learn in Module 4

Section 4.3 The Enhancement Mode MOSFET.

- The IGFET (Insulated Gate FET).
- MOSFET(IGFET) Construction.
- MOSFET(IGFET) Operation.
- MOSFET (IGFET) Circuit Symbols.
- Handling Precautions for MOSFETS

The Insulated Gate FET (IGFET).

The Metal Oxide Silicon FET (MOSFET) or Metal Oxide Silicon Transistor (M.O.S.T.) has an even higher input resistance (typically 10^{12} to 10^{15} ohms) than that of the JFET. In the MOSFET device the gate is completely insulated from the rest of the transistor by a very thin layer of metal oxide (Silicon dioxide SiO_2). Hence the general name applied to any device of this type, is the IGFET or Insulated Gate FET.

Planar Technology.

There are several ways in which an insulated gate transistor may be constructed. All the methods used however, make use of planar technology in which the various parts of the device are laid down as planes or layers on the upper surface of a "SUBSTRATE" in a similar way to that shown on the Planar Transistors page in the BJT section.

The layers are laid down one by one, by diffusing various semiconductor materials with suitable doping levels, as well as layers of insulation into the surface of the device, under carefully controlled conditions at high temperatures. Parts of a layer may be removed by etching, using photographic masks to make the required pattern of the electrodes etc. before the next layer is added. The insulating layers are made by laying down very thin layers of silicon dioxide and conductors are created by evaporating a metal, such as aluminium on to the surface. The transistors produced in this way have a much higher quality than is possible using other methods, and many transistors can be produced at one time on a single slice of silicon, before the silicon slice is cut up into individual transistors or integrated circuits.

MOSFET (IGFET) Construction.

The basic construction of a MOSFET is shown in Fig. 4.3.1. A body or substrate of P type silicon is used, then two heavily doped N type regions are diffused into the upper surface, to form a pair of closely spaced strips.

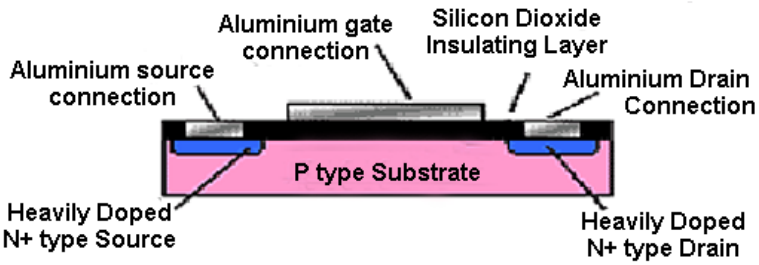

Fig. 4.3.1 N Channel Enhancement Mode MOSFET Construction

A very thin (about 10^{-4} mm) layer of silicon dioxide is then evaporated onto the top surface forming an insulating layer. Parts of this layer are then etched away above the N+ type regions using a photographic mask to leave these regions uncovered. On top of the insulating layer, between the two N type regions, a layer of aluminium is deposited. This acts as the GATE electrode. Metal contacts are also deposited on the N+ type regions, which act as the SOURCE and DRAIN connectors.

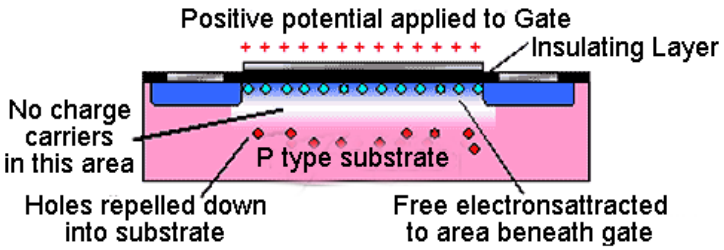

Fig. 4.3.2 N-Channel Enhancement Mode MOSFET Operation.

MOSFET (IGFET) Operation.

The gate has a voltage applied to it that makes it positive with respect to the source. This causes holes in the P type layer close to the silicon dioxide layer beneath the gate to be repelled down into the P type substrate, and at the same time this positive potential on the gate attracts free electrons from the surrounding substrate material. These free electrons form a thin layer of charge carriers beneath the gate electrode (they can't reach the gate because of the insulating silicon dioxide layer) bridging the gap between the heavily doped source and drain areas. This layer is sometimes called an "inversion layer" because applying the gate voltage has caused the P type material immediately under the gate to firstly become "intrinsic" (with hardly any charge carriers) and then an N type layer within the P type substrate.

Any further increase in the gate voltage attracts more charge carriers into the inversion layer, so reducing its resistance, and increasing current flow between source and drain. Reducing the gate source voltage reduces current flow. When the power is switched off, the area beneath the gate reverts to P type once more.

As well as the type described above, devices having N type substrates and P type (inversion layer) channels are also available. Operation is identical, but of course the polarity of the gate voltage is reversed.

This method of operation is called "ENHANCEMENT MODE" as the application of gate source voltage makes a conducting channel "grow"; therefore it enhances the channel. Other devices are available in which the application of a bias voltage reduces or "depletes" the conducting channel. These are described on the Depletion Mode MOSFET page.

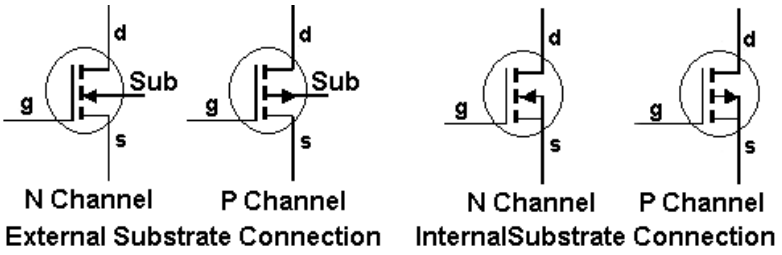

Fig. 4.3.3 Circuit Symbols for Enhancement Mode MOSFETs (IGFETs)

Handling Precautions.

In operation, although the gate has a voltage applied to it, no gate current flows because of the silicon dioxide layer beneath the gate terminal. One well known problem exists regarding this layer however. Although silicon dioxide is an excellent insulator, the layer used on a MOSFET is extremely thin, and therefore can be permanently damaged if a high voltage is applied across it. It will break down just as any other insulator will. Because it is so very thin, it does not need very high voltages to cause total breakdown, and as the gate has such a very high resistance, any voltage present will not be reduced by current flow.

Therefore voltages due to static electricity, which are present all the time in almost any environment, and may reach several thousand volts if no current is drawn to discharge them, present a threat to the insulating layer. For this reason it is wise to transport FETs in special conductive packaging so that no voltage can build up between any of the terminals of the device. Once the transistor is connected into a circuit, the components of the circuit should afford sufficient protection by forming conducting paths around the device, so preventing the build up of high static voltages. In most modern devices special protection diodes are built in to the device to give some protection against static damage. This protection is limited however, and manufacturers handling instructions should be studied before handling any MOS device.

An informative Data Sheet "Handling Instructions and Protection against Electrostatic Discharges" is produced by the Microsemi Corporation and is available via our Links page.

Module 4.4

Depletion Mode MOSFETs.

What you'll learn in Module 4

Section 4.4 The Depletion Mode MOSFET.

- Depletion Mode MOSFET Operation.
- MOSFE (IGFET) Circuit Symbols.
- Applications of MOSFETS
- High Power MOSFETS

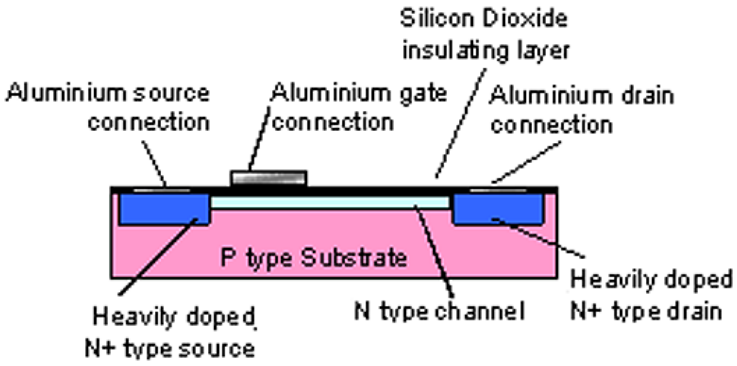

Fig.4.4.1 Depletion Mode N Channel MOSFET

N Channel Depletion Mode MOSFET

The depletion mode MOSFET shown as a N channel device (P channel is also available) in Fig. 4.4.1 is more usually made as a discrete component, i.e. a single transistor rather than IC form. In this device a thin layer of N type silicon is deposited just below the gate-insulating layer, and forms a conducting channel between source and drain.

Therefore when the gate source voltage V_{GS} is zero, current (in the form of free electrons) can flow between source and drain. Note that the gate is totally insulated from the channel by the layer of silicon dioxide. Now that a conducting channel is present the gate does not need to cover the full width between source and drain. Because the gate is totally insulated from the rest of the transistor this device, like other IGFETs, has a very high input resistance.

Depletion Mode Operation

In the N channel device, shown in Fig. 4.4.2 the gate is made negative with respect to the source, which has the effect of creating a depletion area, free from charge carriers, beneath the gate. This restricts the depth of the conducting channel, so increasing channel resistance and reducing current flow through the device.

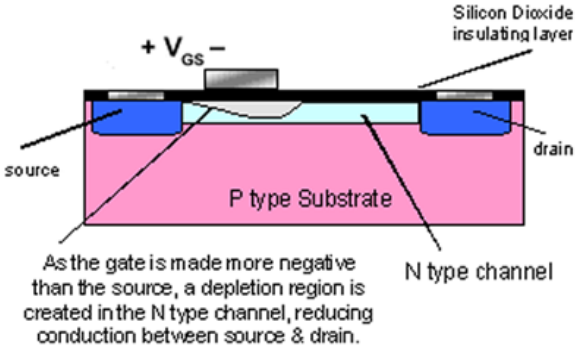

Fig.4.4.2 N channel depletion mode MOSFET operation

Depletion mode MOSFETS are also available in which the gate extends the full width of the channel (from source to drain). In this case it is also possible to operate the transistor in enhancement mode. This is done by making the gate positive instead of negative. The positive voltage on the gate attracts more free electrons into the conducing channel, while at the same time repelling holes down into the P type substrate. The more positive the gate potential, the deeper, and lower resistance is the channel. Increasing positive bias therefore increases current flow. This useful depletion/enhancement version has the disadvantage that, as the gate area is increased, the gate capacitance is also larger than true depletion types. This can present difficulties at higher frequencies.

Depletion Mode MOSFET Circuit Symbols

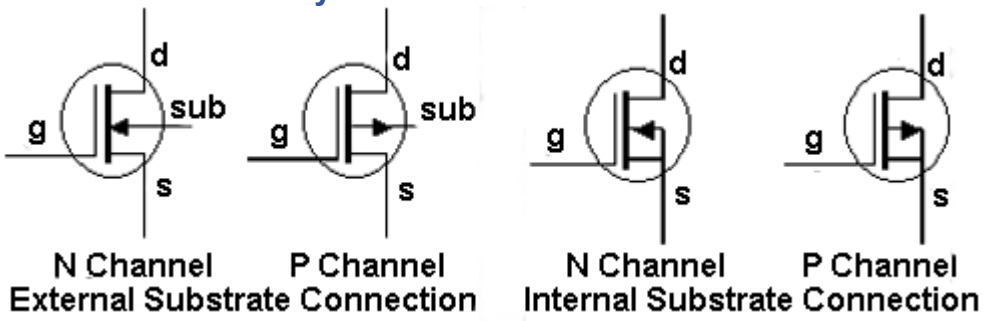

Fig.4.4.3 Circuit Symbols for Depletion Mode MOSFETs (IGFETs)

Notice the solid bar between source and drain, indicating the presence of a conducting channel.

Note: Making the gate more negative reduces conduction between source and drain In N channel devices, but increases conduction between source and drain In P channel devices.

Applications of FETs

Although FETs have a lower gain than bipolar transistors, their very high input impedance makes them suitable for applications where input signals may be severely reduced if applied to a bipolar transistor base that needs base current to operate. The planar technology used to make FETs is the same as that used to make integrated circuits, so most of the transistors found in I / Cs are of this type. A useful feature of FETs is that they tend to produce less background noise than Bipolar types and so are useful in the initial stages of systems such as amplifiers; radios etc. where signal levels are very small and could be swamped by excessive background noise.

High Power FETs

FETs used in high power output stages are often seen referred to as VMOS, DMOS or TMOS. These transistors are basically the same as other IGFETs but have specialised constructions that allow them to pass currents as large as 10A. They are also able to switch on and off very quickly (in nano seconds). This allows them to be used in such circuits as switch mode power supplies where very fast switching is essential.

Module 4.5
Power MOSFETs

What you'll learn in Module 4.5

After studying this section, you should be able to:

- Understand the operation of Power MOSFET switches.
- Recognise important characteristics of Power MOSFETS
- Choose appropriate Power MOSFETs for switching DC current.
- Describe typical driver circuits for power MOSFETS in switching and controlling high current loads

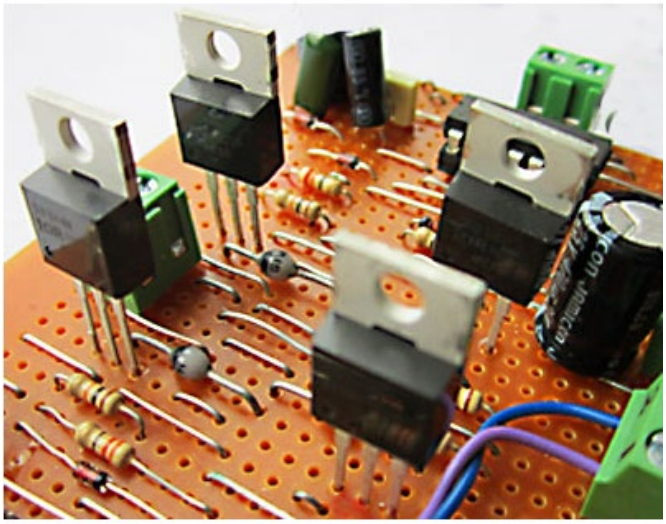

Fig. 4.5.1 Power MOSFETs

The Power MOSFET as a Switch

Both N and P channel Power MOSFETs (though mainly N channel) are widely used for switching DC loads of many types. They form the essential link between low power electronics and higher power 'real world' applications. Over recent years their use has grown enormously, replacing electro-mechanical relays to switch electrical loads in many applications. The load is switched on by applying a small voltage potential difference between the MOSFET Gate and Source, the actual value and polarity of this voltage depends on the MOSFET type chosen. When the MOSFET is used as a switch, it operates in 'saturation mode' and so conducts heavily when switched on. Because the current between Source and Drain (V_{DS}) will be high, the resistance of the Drain to Source channel must be very low. Therefore if the power dissipated by the MOSFET, (and so its temperature) is to remain low, the resistance of the channel must typically be just a few milli-Ohms at a typical ambient temperature of 25°C. However this extremely low resistance will increase at higher temperatures.

The MOSFET vs a Relay

Unlike a mechanical relay or switch that has contacts either completely open or completely closed, a Power MOSFET provides an extremely high (but not infinite) resistance when in its 'off' mode, or an extremely low (but not zero) resistance (R_{DSon}) when in its 'on' mode. The MOSFET is therefore basically a resistor whose value can be controlled by a small change in Gate/Source voltage (V_{GS}). The actual value of the resistance between Drain and Source whilst the MOSFET is switched on is called R_{DSon}. This is an important value because the Power MOSFET is designed to switch relatively large amounts of current and so whether it is 'on' or 'off' there will always be some resistance present, which will cause the MOSFET to dissipate some power as heat, and too much heat, (usually above 150 to 175°C) will be very likely to destroy the MOSFET.

Fig. 4.5.2 Relay vs MOSFETs

Choosing a Power MOSFET

To ensure that this does not happen, having a clear understanding of the relationships beween Voltage, Current, Resistance and Power to enable selection of a suitable Power MOSFET for a particular application is important. There are hundreds of different types of Power MOSFETs produced by many manufacturers so selection can be difficult. Some power MOSFET designs are aimed at particular markets, for example high frequency switched mode power supplies need MOSFETs with a very high switching speed. Alternatively, computer driven control systems may require MOSFETs that have a lower than usual gate turn-on voltage to interface simply with 5V or 3.3V logic systems. Within each of these sub-groups there will be a choice of pin-out design. Surface mount types such as the D-PAK are often the most likely first choice but many types are still available in TO-220 packages as shown in Fig. 4.6.1. Making a reasoned choice for any application is a matter of studying a range of possible data sheets to identify suitable values for each of the following criteria.

Maximum Drain/Source Voltage (V_{DS})

This is normally one of the 'headline' criteria on many data sheets. Some high values for V_{DS} are often claimed but it is important to remember that this figure is the absolute maximum voltage that the MOSFET can withstand between Drain and Source when in the 'off' condition. It is therefore generally considerably higher than the actual working voltage you would expect your chosen MOSFET to experience under normal working conditions, remember that with power switching applications there could always be the chance of unexpected voltage spikes etc. V_{DS} should therefore be considered as a guide to long term reliability rather than a working voltage. As a rule of thumb the working voltage applied across Drain and Source should be no more than 80% of the maximum V_{DS}.

Gate/Source Voltage (V_{GS})

The voltage applied between Gate and Source of a Power MOSFET to cause conduction between Source and Drain has two relevant values, firstly $V_{GS(th)}$ also called the Gate threshold voltage. This is a voltage applied to the Gate that will cause a current of 250µA to flow between Drain and Source. This is not intended to indicate a minimum turn on voltage, but is the voltage level the the Gate should be kept **below** while the MOSFET is held in its 'off' state. This minimises any leakage current between Source and Drain. To turn the MOSFET on the Gate/Source voltage should be considerably higher than $V_{GS(th)}$ but lower than the maximum allowed value for V_{GS}. This maximum value may be a range of several volts, e.g. ±20V and is normally quoted in the data sheet for any particular MOSFET. In MOSFETs classed as 'Logic Level' the Gate/Source voltage will be +5V or less but in MOSFETs without this designation V_{GS} will be higher. The ideal value chosen for a particular MOSFET will cause the Drain/Source Resistance (R_{DSon}) to drop to a value that generates the minimum amount of wasted heat in the MOSFET whilst it is conducting.

Drain/Source Resistance (R_{DSon})

R_{DSon} is one of the headline characteristics of MOSFETs and is crucial in designing switching circuits using Power MOSFETs. The greater the value of R_{DSon} the more heat will be generated for a given value of Drain/Source current, therefore the lower the value of R_{DSon}, the better. The value of R_{DSon} also depends to some degree on Gate/Source voltage (V_{GS}) and so manufactures will often quote several R_{DSon} values for different operating conditions. Selecting the appropriate value of R_{DSon} is the starting point in calculating the safe operating conditions in the design of a Power MOSFET switch circuit. Its value is greatly influenced by the Gate-Source Voltage (V_{GS}), to much lesser extent by the Drain Current, but is closely linked to the temperature generated in the MOSFET.

Maximum Drain Current (I_D)

Manufacturers usually quote the maximum drain current as one of their headline characteristics but it is important to remember that the headline maximum value is not normally a practical value but the maximum current under ideal cooling solutions with perfect thermal properties and the MOSFET on the verge of thermal breakdown. A more practical value for I_D would be one related to calculated operating conditions that will keep the temperature of the MOSFET, (with or without a heat sink), below the maximum operating temperature, which is usually between 150°C and 175°C. Examples of typical calculations are given below.

Thermal Resistance (R_{thJC})

This characteristic describes the thermal resistance in degrees Celsius(°C) or degrees Kelvin(°K) per Watt of power dissipated between the transistor junction and the transistor case; for example 1.6 °K/W describes by how much the junction temperature of the MOSFET (in degrees Kelvin) will rise for every Watt of power dissipated. Various measures of Thermal Resistance can be used, depending on the type of device (transistor, MOSFET, IC etc.) to describe how efficiently the heat generated at a PN junction is transferred between the junction and the case, (subscript JC), between the junction and the air surrounding the Device (subscript JA) or, if a heat sink is used the different °K/W figures for each section of pathway across which heat is dissipated can be added to achieve a measure of the cooling efficiency; see more on heat sinks here. In many modern circuits where surface mount MOSFETS may be used different figures for R_{thJC} may be used depending on the way the MOSFET is mounted, for example on a an area of copper print on the PCB or on a standard size of specifically designed PCB (e.g. a single layer 40mm square of flame retardant (FR-4) PCB mounted vertically in still air).

Typical Calculations for Using a MOSFET

When considering using a MOSFET as a switch, the amount of heat generated at its PN junctions is an important factor affecting the operation of the circuit and whether excessive temperature may affect its reliability. An example of how such calculations may inform the design of a circuit is given below, where a IRFZ44N MOSFET from International Rectifier (now Infineon) is used as a switch, to drive a 12V 36W automotive headlamp bulb from 5Vpp logic PWM signal. Although the MOSFET in this example is not suitable to be driven directly from a logic level input, the 12V 3A ouput circuit is totally isolated from the logic input via a 4N25 Opto Isolator which not only protects the input circuit, but also provides a 9Vpp square wave sufficient to drive the MOSFET gate.

The circuit providing a logic level output to drive the 4N25 in this case could be an Arduino running a simple pulse width modulation program that continually alters the brightness of the lamp, or a Pulse Width Modulator circuit based on discrete components including a 555 timer. The circuit, shown in Fig. 4.6.2 easily drives the 3A resistive load without any excessive heating.

The circuit could possibly drive higher current loads with or without adding a heat sink but since 12V at 3A is also the limit of my bench power supply, further investigation was not possible.

The Power MOSFET Drive circuit requires a series of choices and calculations. The MOSFET chosen to control the brightness of a 12V DC incandescent lamp is based on the following criteria:

1. The Maximum V_{DS} voltage of the MOSFET must be greater than 12V by a margin to allow for any supply voltage variations, so a MOSFET with a maximum DC voltage of 55V seems reasonable.

2. A low R_{DSon} value is important to prevent excessive heating of the MOSFET.

3. As the MOSFET is to be driven from a logic circuit via 4N25 opto-isolator, logic compatibility is not needed. However if isolation is not a priority, a similarly specified MOSFET can be used, but it must be compatible with a logic level drive.

4. The package type should be available as a through hole mounting TO-220 as the prototype is to be built on strip-board.

Starting with these basic criteria in mind, the IRFZ44N was chosen. The next task is to check that the chosen MOSFET is up to the job. This requires some calculations based on information gathered from the manufacturer's data sheet.

From the IRFZ44N data sheet:

R_{DSon} (for V_{GS} = 10V) = 17.5mΩ

De-rated by adding 20% = 21mΩ

Power Dissipated = I^2R

Lamp Current (on) = 3A (Supply Voltage = 12V, Lamp Rated Power = 36W)

Power Dissipated in the MOSFET = I^2 x R_{DSon} = 3^2 x 21mΩ = 189mW

Thermal Resistance (junction to case) of the MOSFET with no heat sink (R_{THJC}) =1.5°C per Watt

Therefore estimated junction temperature with Ambient Temperature (T_A) =25° = (1.5 x R_{THJC}) + T_A

= (1.5 x 189 E^{-3}) +25 = **25.28°C**

Therefore as maximum safe operating temperature for the IRFZ44N is 175°C (or °K) and the forecast rise in Junction Temperature is only 0.28°C (25°C to 25.28°C) the MOSFET can be safely operated without a heat sink. However these calculations are based on the MOSFET alone and do not wholly take into consideration the effect of the external components and how they interface with the MOSFET. Working examples of this design process and how it can be applied to practical switching circuits are described in Module 4.6 MOSFET Switches.

Module 4.6
MOSFET Switches

What you'll learn in Module 4.6

After studying this section, you should be able to:

- Understand the operation of Power MOSFET switches.
- Recognise important characteristics of Power MOSFETs.
- Choose appropriate Power MOSFETs for switching DC current.
- Describe typical driver circuits for power MOSFETs in switching and controlling high current loads.
- Recognise typical safety measures to prevent damage due to over heating, over voltage or over current.

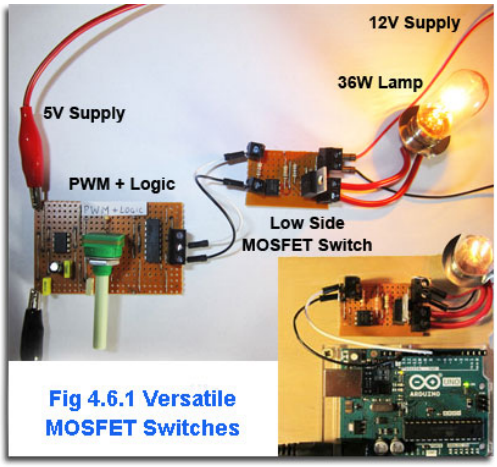

Fig 4.6.1 Versatile MOSFET Switches

Building MOSFET Switches

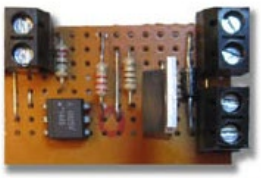

Fig. 4.6.2 The MOSFET Switch

To test the calculations made in Module 4.5, the circuit shown in Fig. 4.6.2 was built on strip board (proto-board). Only a few components are needed and the circuit also incorporates an opto-isolator to isolate any logic input circuit from the high current high voltage output that the switch may be controlling.

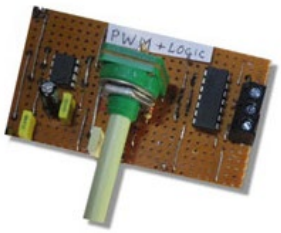

Fig. 4.6.3 PWM+Logic Signal Source

The MOSFET switch circuit load in this case is a 12V 36Watt automotive headlamp bulb and the input to the MOSFET switch will be a pulse width modulated, logic level signal. This may be supplied by any 5V compatible logic circuit producing a PWM signal at a frequency in the high audio frequency range. In initial tests the N Channel MOSFET Low Side switch was connected to a Pulse Width Modulated (PWM) + Logic circuit based on a modified version of the single 555 timer design (Fig. 4.4.8) in the Learnabout-Electronics Oscillators section where a description of its operation can be found. For these tests, a Schmitt inverter was added to ensure fast rise and fall times to the resulting PWM output signal. You can download full construction details for the PWM circuit here.

Alternatively the variable PWM input signal could be obtained from any circuit having a 5V logic output, such as the Arduino as shown in Fig 4.6.9, in this case running the simple PWM sketch, which continually dims and brightens the lamp.

The circuit diagram for the switch is shown in Fig. 4.6.5 and the layout for initial tests is in Fig. 4.6.1.

See the tests in action at www.learnabout-electronics.org

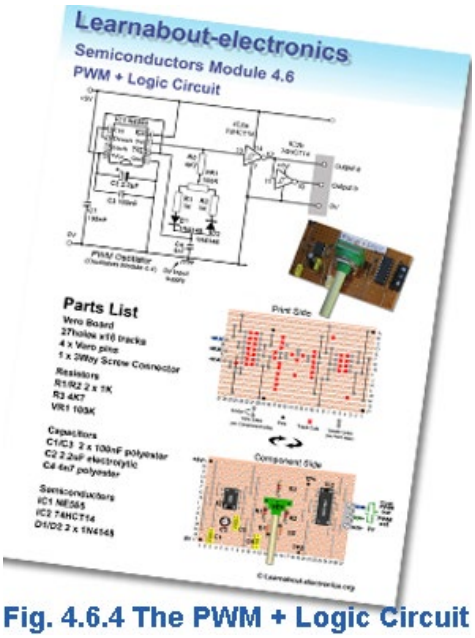

Fig. 4.6.4 The PWM + Logic Circuit

Pulse Width Modulation Sources

Two outputs are available from the PWM circuit, which are the actual PWM signal and an inverted version. Either can be applied to the input terminals of the MOSFET circuit. For testing, the output of the MOSFET switch was connected to a 36-Watt load (an automotive headlamp bulb) connected between the 12V lamp supply and the Drain terminal of the MOSFET Switch as shown in Fig 4.6.5. This represents the 3A maximum load the circuit is designed for, as 3A is also a common maximum current available from bench power supplies.

The PWM input signal can also be obtained from any circuit having a 5V logic output, such as the Arduino as shown in Fig 4.6.8, in this case running the simple PWM sketch, which continually dims and brightens the lamp.

The operation of the Pulse Width Modulator circuit is based on the 555 circuit described in Oscillators Module 4.4. For use as a MOSFET driver, the circuit has been slightly modified to increase its frequency of operation, as when it is used for driving loads such as DC Brushed motors the frequency of operation needs to be high enough to avoid causing an audible whine, as the inductive nature of the motor can make it operate as a loudspeaker at low frequencies. The action of the opto-isolator is also described in Semiconductors Module 5.2.

A MOSFET Switch Circuit

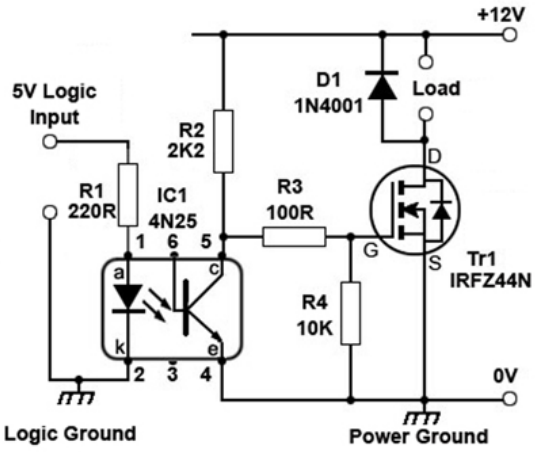

Fig. 4.6.5 The MOSFET Switch With Isolated Input

The opto-isolator (IC1) and its two resistors R1 and R2 are not absolutely essential to the operation of the MOSFET but are highly desirable because the complete circuit makes a very useful self contained switch, suitable for interfacing many low voltage, low current electronics projects to higher voltage/current peripherals. IC1 performs two functions; it isolates any external driving circuit from the MOSFET and also increases the amplitude of a 5V logic signal sufficiently to drive a standard (i.e. not logic input version) MOSFET without the need for an additional amplifier. The purpose of R3 is to prevent or dampen any ringing that may be caused by the combination of the gate capacitance and the inductance of any wiring, especially in drive circuits working at high frequencies, where this is more important when driving higher frequency circuits such as switched mode power supplies. A Typical value for R3 would be 100Ω or less as higher values can slow down switching.

It is Essential when switching MOSFETs that the switching time between the off and on states is kept as short as possible. When the MOSFET is Fully switched on (saturated) The Drain-Source Voltage is close to zero, so although there may be a large current flowing, the power dissipated (I^2R) is very small. When the MOSFET is switched off there will be a large voltage between Drain and Source but practically no current is flowing so again the power dissipated in the MOSFET is practically zero Watts. However during the changes between on and off, both voltage and current will be considerable and so large amounts of power will be dissipated for a very short time. Therefore the quicker the MOSFET can be switched on or off the less power will be dissipated. The total power dissipated during each operating cycle will be approximately the sum of the dissipation during each of the off-to-on and on-to-off periods.

R4 ensures that as the MOSFET switches off when the positive gate drive signal is removed, the gate capacitance is discharged immediately to zero volts rather than remaining close to the switch on level, so reducing the probability of random switch on of the MOSFET. D1 is connected across the load terminals to prevent damage to the MOSFET due to back emf when used with inductive loads.

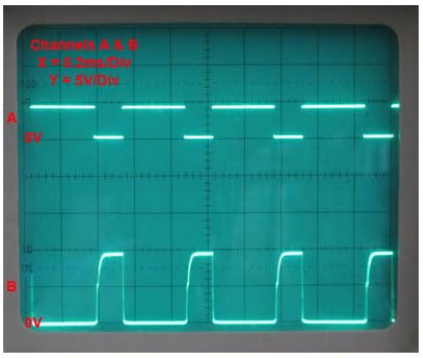

Fig. 4.6.6 4N25 Opto-isolator Waveforms

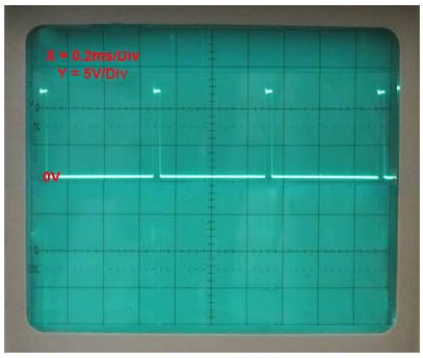

Fig. 4.6.7a Drain Waveform at Minimum Power

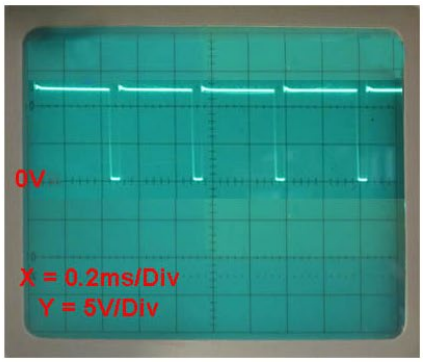

Fig. 4.6.7b Drain Waveform at Maximum Power

Looking at the switching action of the MOSFET, it can be seen from the waveforms in Figs. 4.6.6 and 4.6.7 a and b. Notice in Fig. 4.6.6 that there is some curvature to the rising voltage in waveform B (the opto-isolator output), which tends to slow down the switching. This is due to the relatively slow switch on time (compared with the operating frequency) of the opto-isolator. However, looking at the drain waveforms in Figs. 4.6.7 a and b this has not adversely affected the switch on time of the MOSFET as the curvature in the opto-isolator output waveform is mainly in the upper voltage levels of the 10Vpp gate signal, after the MOSFET has already switched on. Note that the 4N25 opto-isolator is not rated as particularly fast; there are a number of faster devices, which use opto diodes instead of opto transistors as the output component, however they do tend to cost more and are more likely to be used in higher frequency systems.

Temperature Tests

On testing the temperature rise for the whole circuit used in Figs. 4.6.8 and 4.6.9 it was found that although the calculations suggested a temperature rise only very slightly above 25°C would be achieved, the completed circuit shown in Fig. 4.6.9 actually ran at a maximum temperature of around 28°. Higher than the calculations suggest, but still well within safe limits when using a 3A motor as the load. With the circuit connected to the 36Watt lamp however, as shown in Fig. 4.6.8, the temperature rise was considerably higher, rising to around 37°C, this appeared to be due in some part to the lamp (very hot) being so close to the MOSFET and therefore raising the ambient temperature. The MOSFET temperature dropped back, close to 29° when a small sponge shield was placed between the lamp and the MOSFET.

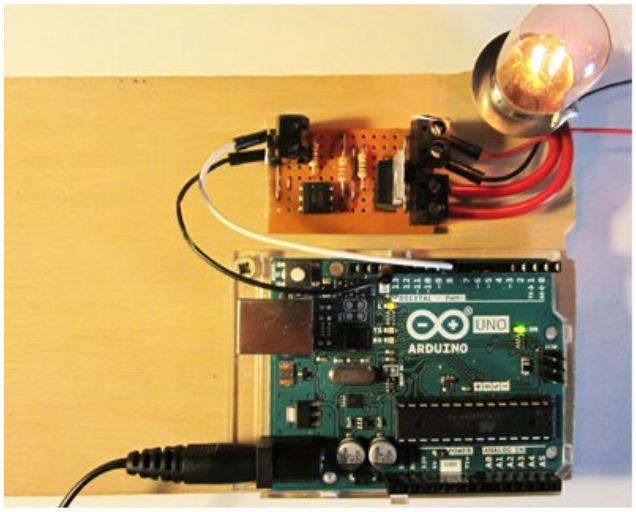

Fig. 4.6.8 Arduino Driving a 36 Watt Lamp.

Fig. 4.6.9 Arduino & a 3A DC Motor.

The switch therefore worked well with both resistive (12V lamp) and inductive (brushed DC motor) loads upto 3A when driven from a 12V supply with an input from a 5V logic source. The input signal was provided by either a simple pulse width modulator circuit or the Arduino.

The circuit also performed well with the MOSFET replaced by a 039N04L logic level MOSFET. In this case it would not be strictly necessary to use the 4N25 opto-isolator to boost the logic input level to the 10Vpp needed by the IRFZ44N, but then the input circuit would be exposed to any fault condition in the MOSFET circuit. The extra expense in using an opto-isolator compared with a wrecked Arduino is therefore justified.

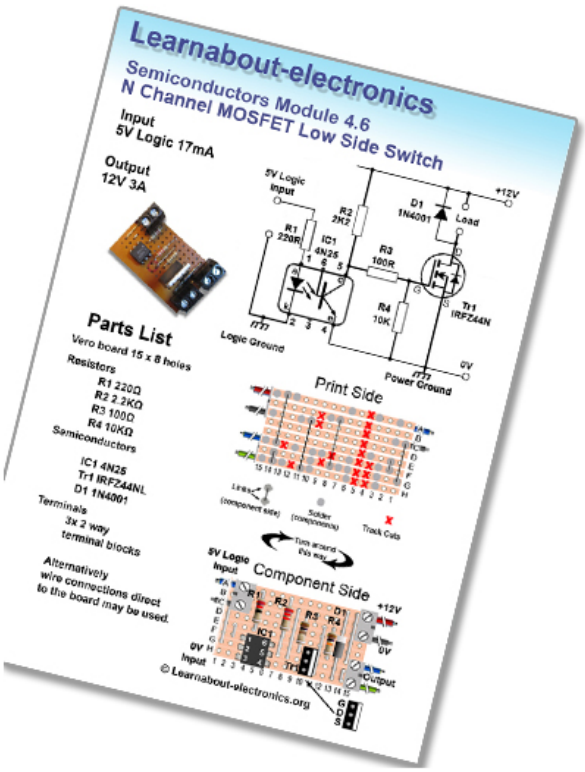

Fig. 4.6.10 Build an N Channel MOSFET Low Side Switch Click image to download

High Side and Low Side Switching

The MOSFET in the above example is placed between the load and ground, this method of operation is therefore called Low Side Switching and is a simple and much used method of using MOSFET switches. However there are some applications where this may not be suitable, as when the load requires a ground connection in common with other load devices. Also when the MOSFET is 'off' and current through the load ceases, the voltage at Point X in Fig. 4.6.11a will be at the supply voltage. Whilst this may not be a problem at low voltages, MOSFETs can be used to switch high voltage circuits where having a high voltage present on an apparently inactive circuit can be a safety problem by creating a shock hazard. To eliminate either of these problems, High Side Switching can be used, as shown in Fig. 4.6.11b. where, when the MOSFET switches off the voltage across the load (and at point X) will be at zero volts, (providing that the MOSFET does not develop a short circuit fault).

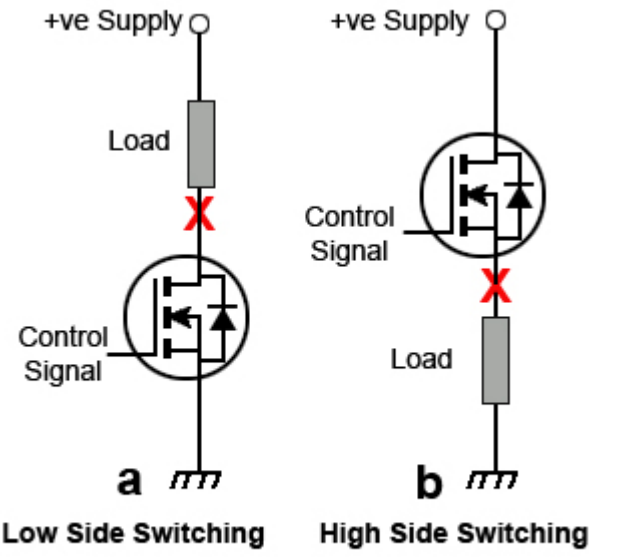

Fig. 4.6.11 Low and High Side Switching

Low side switching is simple to implement using N channel Power MOSFETs but High Side Switching raises some difficulties. The main problem that must be overcome is that the gate voltage (V_{GS}) on an N channel MOSFET must be more positive than the Source voltage in order to switch the MOSFET on. While the MOSFET is off in a high side circuit the Source voltage will be virtually zero volts so the Gate could switch the MOSFET on, but once it is on, the Source voltage will be almost the same as the Drain voltage due to the very low resistance of the conducting MOSFET. As the supply voltage (and now also the source voltage) is likely to be the highest voltage in the circuit, the Gate voltage cannot be made higher than the Source voltage and control is lost.

The High Side MOSFET Switch

To make High Side Switching possible there are a number of methods that can be used. The simplest of these is to replace the N channel MOSFET with a P channel type. The circuit symbols for each are shown in Fig. 4.6.12. The only difference in these symbols is the direction of the arrow indicating the channel; in the P channel MOSFET the arrow now points away from the P type channel.

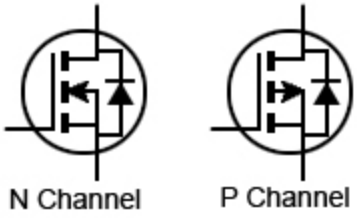

Fig. 4.6.12 N & P Channel Enhancement MOSFETs

However the connection of the P channel MOSFET compared with the N channel is reversed, The P channel source is connected to the positive supply and the gate must now be connected to a lower voltage that the source in order for the MOSFET to switch on. The drain is now connected to the more positive side of the load, and the load's negative terminal is connected to ground.

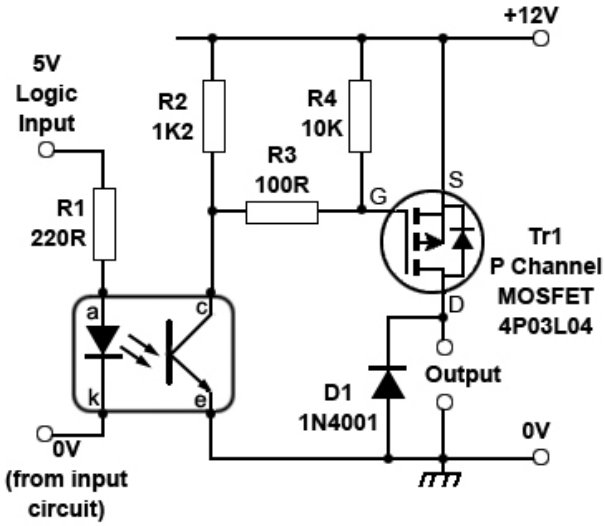

Fig. 4.6.13 P Channel High Side Switch

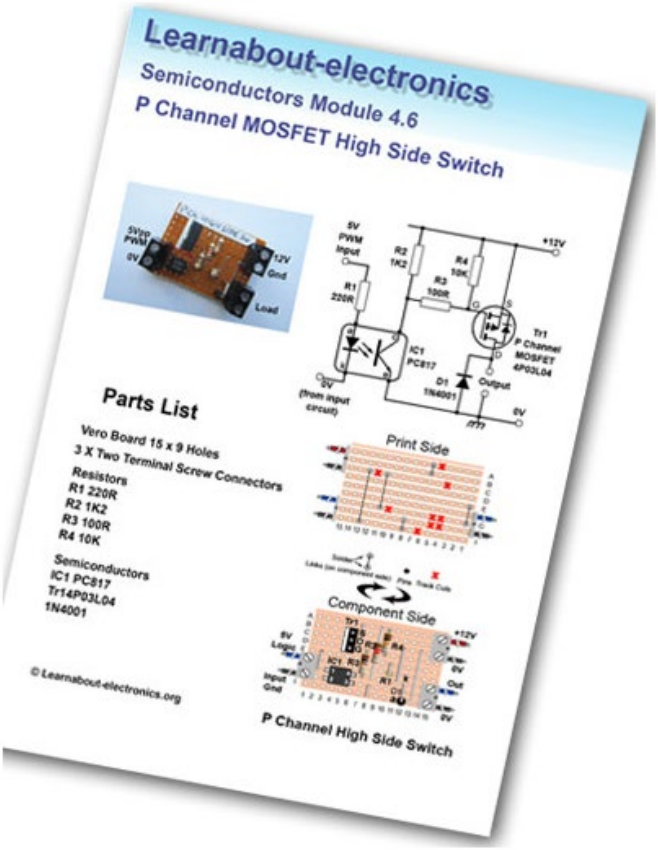

Fig. 4.6.13a Build a P Channel MOSFET High Side Switch Click image to download

A circuit for a typical high side switch using a P channel MOSFET is shown in Fig. 4.6.13. Notice the similarities and differences between Figs. 4.6.13 and 4.6.5. Firsly in Fig.4.6.13 the resistor R4 whose purpose is to discharge any remaining potential on the gate at switch off is now connected to the positive supply rail instead of to ground. This indicates that the gate potential, when switched on will be more negative than supply providing a negative value of V_{GS}.

Fig. 4.6.13 also uses a different opto-isolator, a PC817 instead of the 4N25 in Fig. 4.6.5. This is not an important difference as a number of similar isolators could be used, it just needs to have a reasonable 12Vpp output waveform to switch the MOSFET Gate. The MOSFET used in the this high side switch is a logic level 4P03L04 from Infineon and as it only needs its gate to be 4.5V lower than the 12V supply, the 12Vpp waveform applied to its gate easily switches the MOSFET on or off.

The P Channel High Side Switch therefore solves the problem of using an N Channel MOSFET for high side switching; however this 'cure' can also have some side effects. P channel MOSFETs generally have a higher R_{DSon} compared to N type MOSFETs having a similar internal chip size. This means that during the time when the MOSFET is on, a P type MOSFET will produce more

heat than a similar N type device. This is especially relevant in high current circuits. However as this module restricts itself to relatively low power circuits the difference in R_{DSon} values is less of a concern. For example the P channel 4P03L04 has an R_{DSon} value of 4.4mΩ whereas the N channel IRFZ44N has a R_{DSon} value of 17.5mmΩ. Despite this the section below describes a method for using an N channel MOSFET in a high side switch circuit.

The N Channel High Side Switch

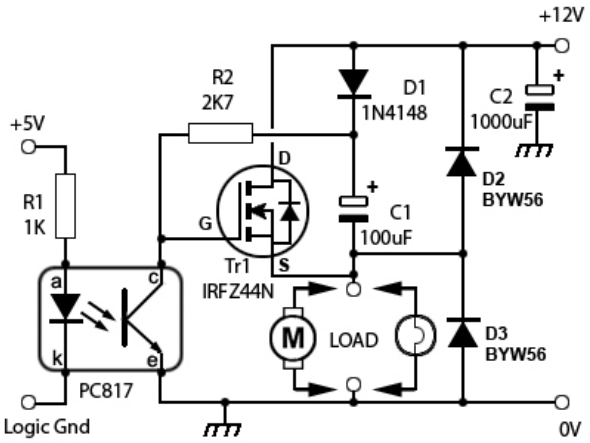

Fig. 4.6.14 N Channel High Side Switch

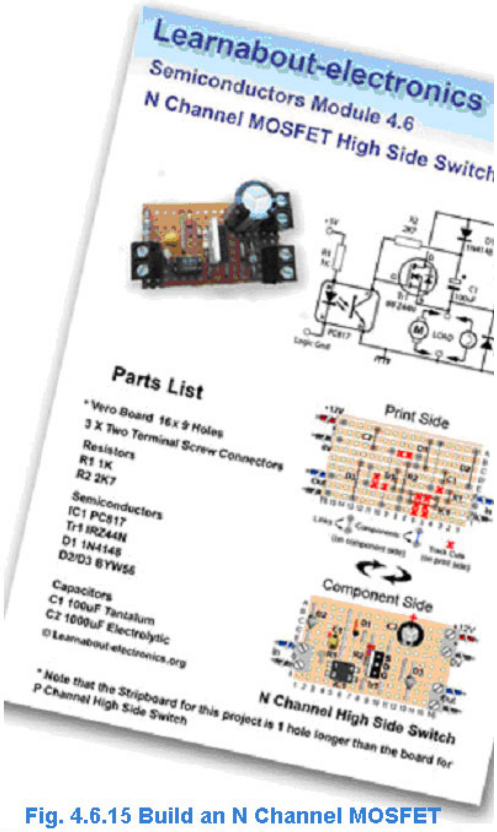

Fig. 4.6.15 Build an N Channel MOSFET High Side Switch. Click Image to Download

The main problem in using an N channel MOSFET in a high side switch is that in order for the MOSFET to switch on, once it has been switched off is that the voltage on the gate terminal of the MOSFET must be made higher than the source voltage, which, as the MOSFET is "off" will be at supply voltage Vcc.

In order to do this the gate voltage must be 'level shifted' in some way. This technique commonly goes under the name of 'Bootstrapping' (i.e. the mythical ability to lift oneself up simply by pulling upwards on your boot straps) - apart from the impossibility of this task, Bootstrapping is not the most useful name, as there are several techniques used in other non-related circuits that use the same name, generally meaning to lift some value up to a higher than normal level.

In this case the "off" voltage (the lowest voltage of the waveform) at the MOSFET gate needs to be lifted up to at least as high as the supply voltage. For example if a logic level MOSFET is used the minimum gate voltage would be equal to the supply voltage (5V) and the peak gate voltage would need to be 5V higher than the supply voltage Vcc. With non-logic level MOSFETs the minimum gate voltage will need to be at about the supply voltage (e.g.12V) and the peak voltage approximately double the voltage of Vcc. The purpose of bootstrapping is to achieve these increases without an external supply.

This only requires a few extra components, but the system only works for MOSFET circuits that are continuously switched on and off (such as PWM circuits). Circuits that are turned on for long periods require different techniques.

How the Bootstrap Circuit Works

When the output transistor of the opto-coupler is turned on, its collector terminal and the MOSFET gate voltage is pulled down to 0V; The MOSFET is switched off and with the Drain voltage at Vcc (12V), the capacitor C1 charges via the diode D1 to almost Vcc (12V). When the opto-isolator output transistor turns off again, its collector voltage and the MOSFET gate rise to Vcc (12V) and the MOSFET turns on. This however also makes the Source voltage rise to 12V (which without

bootstrapping would instantly turn the MOSFET off again as source and gate would be the same voltage) However as C1 is now charged up to 12V, its negative terminal will be at 12V but its positive terminal will now be 12V + 12V = 24V, (pulling the gate voltage up by its bootstraps!) and reverse biasing the diode D1. So with the gate terminal of the MOSFET now at 24V the MOSFET stays switched on, Eventually of course the capacitor would discharge and the gate voltage reduce towards a level that would cause the MOSFET to turn off again, except for the fact that the input signal is switching on and off continually. So provided that the 'off' time is long enough for the capacitor to recharge during each cycle and the 'on' time is not long enough for C1 to discharge, (which would be a comparatively very long time due to the very high gate resistance) the MOSFET continues to work.

Module 4.7
Field Effect Transistor Quiz

Try this quiz based on field effect transistors. Hopefully it'll be easy. Submit your answers but don't be disappointed if you get answers wrong. All the information you need is on the Semiconductors Module at www.learnabout-electronics.org. Find the right answer and learn about Field Effect Transistors as you go.

1. Which of the following devices is a JUGFET?

    a) Unipolar Junction MOSFET

    b) Bipolar Junction FET

    c) Unipolar Junction FET

    d) Bipolar Junction MOSFET

2. Under what conditions does a JFET pass its maximum current?

    a) The gate voltage is at pinch off.

    b) The gate voltage is at 0V.

    c) $+V_{DS}$ is at saturation level and $-V_{GS}$ is at maximum.

    d) $+V_{DS}$ is at pinch off and $-V_{GS}$ is at 0V

3. What does a typical value of 1.6°K/W indicate in the specifications for a MOSFET?

    a) The maximum permitted temperature for the MOSFET.

    b) The value of thermal resistance between the junction and case of a MOSFET.

    c) A typical value of R_{DSon} for a P channel MOSFET.

    d) The increase in ambient temperature per Watt of power in a MOSFET.

4. What type of device is illustrated in Fig.4.7.1?

    a) An N Channel Depletion Layer MOSFET.

    b) A P Channel Depletion Layer MOSFET.

    c) An N Channel Enhancement Layer MOSFET.

    d) A P Channel Enhancement Layer MOSFET.

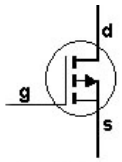

Fig.4.7.1

5. Which semiconductor device is illustrated in Fig.4.7.2?

    a) An N Channel Unipolar JFET.

    b) An N Channel Bipolar Planar JFET.

    c) A P Channel Planar Depletion Mode MOSFET.

    d) A P Channel Unipolar Enhancement Mode MOSFET.

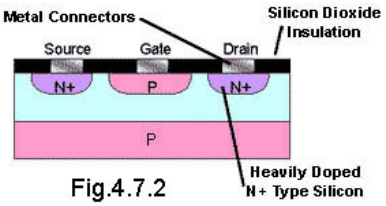

Fig.4.7.2

6. If a MOSFET having a de-rated R_{DSon} value of 21mΩ is passing a Drain/Source current of 3A, what will be the power dissipated by the MOSFET?

    a) 36W

    b) 63mW

    c) 189mW

    d) 25.28mW

7. Fig.4.7.3 shows a JFET Output Characteristic graph. What does the area labelled A indicate?

a) The Cut-off Region.

b) The Ohmic Region.

c) The Pinch-off Region.

d) The Saturation Region.

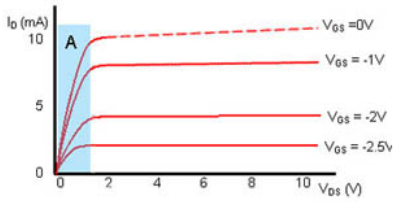

Fig.4.7.3

8. In the circuit shown in Fig.4.7.4, what is the purpose of R4?

a) To discharge the Gate capacitance when the MOSFET switches off.

b) To prevent ringing on the Gate.

c) To prevent over-driving of the gate.

d) To limit over-voltage spikes.

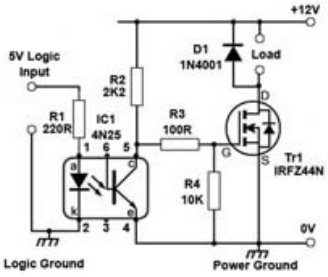

Fig.4.7.4

9. In the circuit shown in Fig.4.7.5, what is the purpose of C1?

a) To remove any AC from the Source terminal.

b) To decouple D1.

c) To prevent any back emf spikes from reaching the gate terminal.

d) To increase the gate voltage V_{GS}.

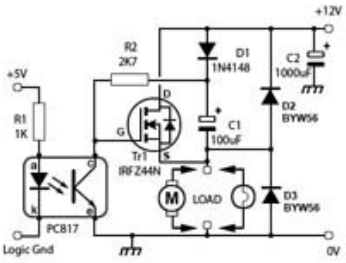

Fig.4.7.5

10. What does the MOSFET characteristic $V_{GS(th)}$ refer to?

a) The maximum threshold for the Gate/Source voltage of a MOSFET in its off state.

b) The ideal Gate/Source voltage for a MOSFET in its on state.

c) The maximum Gate/Source voltage to prevent thermal runaway.

d) A theoretical Gate/Source voltage not achievable in practice.